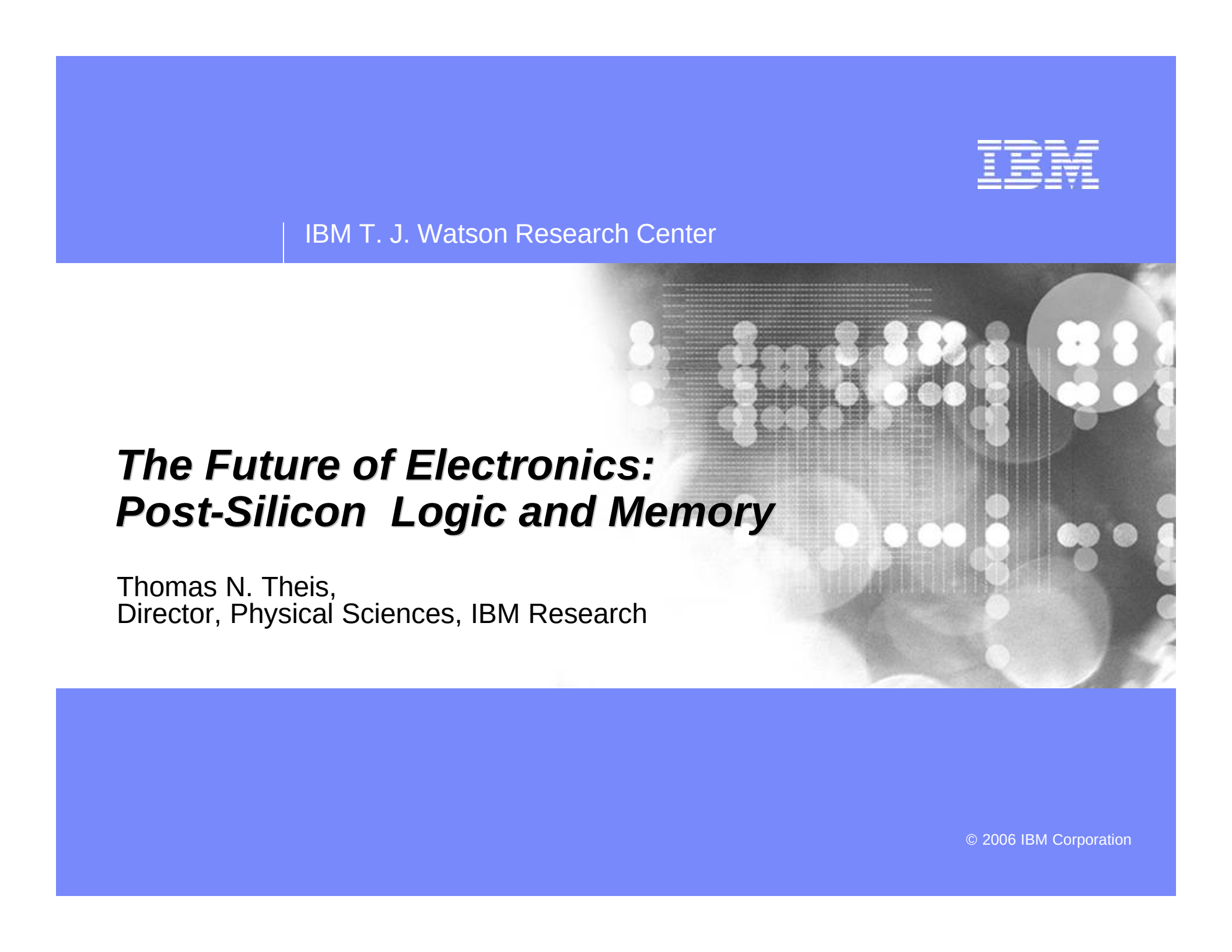
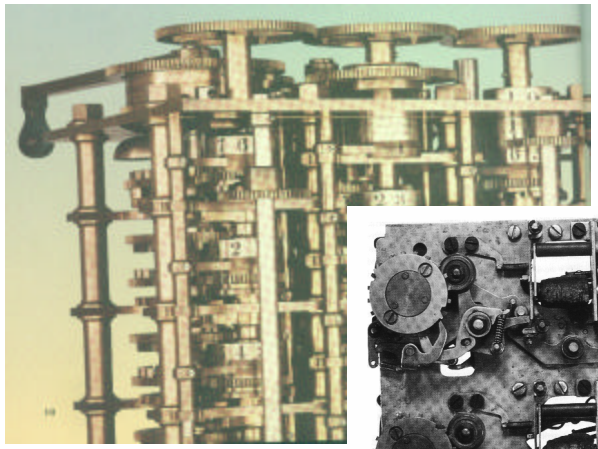


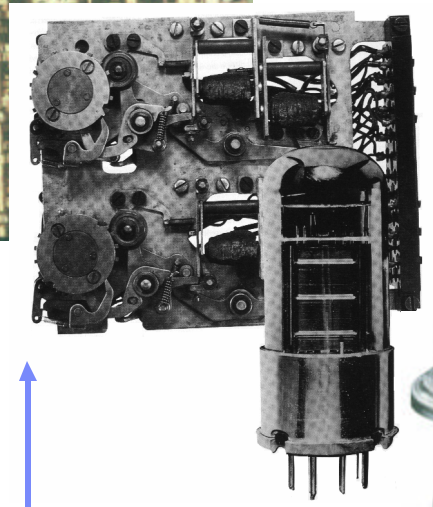
IBM T. J. Watson Research Center

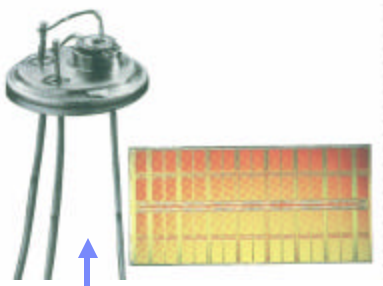
# *The Future of Electronics: Post-Silicon Logic and Memory*

Thomas N. Theis,
Director, Physical Sciences, IBM Research

# Can we extend the IT revolution?







Information technology has progressed through continuous miniaturization and repeated invention of new devices to store, process, and communicate information.

The transistor and other devices are now approaching hard physical limits.

What's Next?

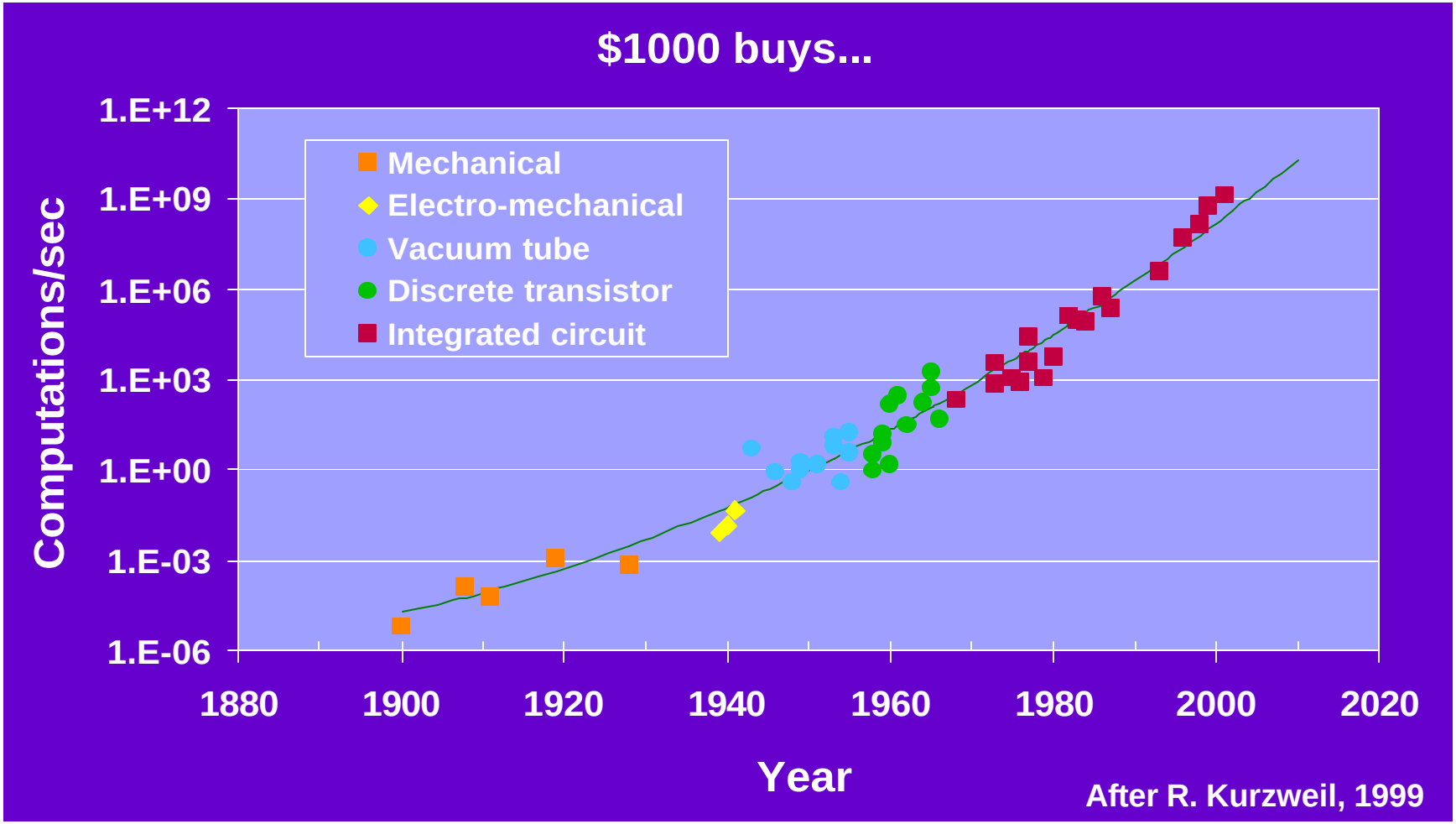
principle features specified to: ℋ1mm

ℋ10 λm

ℋ100 nm

Organic Electronics?
Moletronics?
Spintronics?
Plasmonics?
Quantum Computing?
…?

# Result: Ever-Decreasing Costs of Computation, Ever-Expanding Applications of Information Technology



# Needed: New Devices Based on New Materials and New Physics.

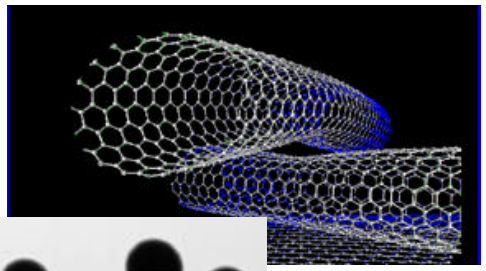
Carbon nanotubes

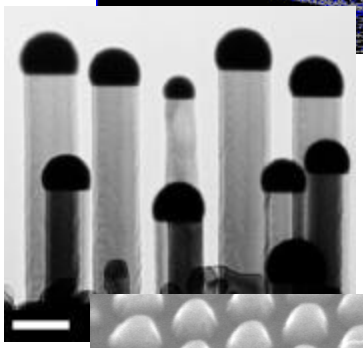
Semiconductor nanowires

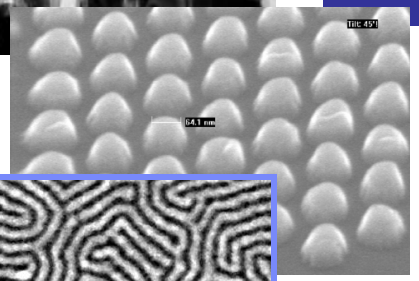
Chalcogenides

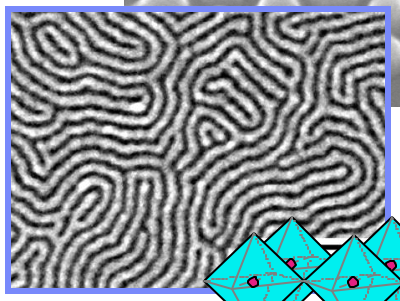
Polymers

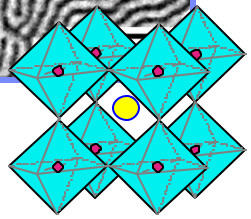
Complex Oxides



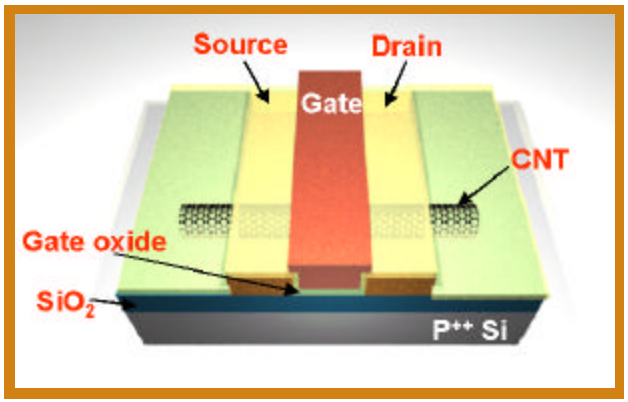


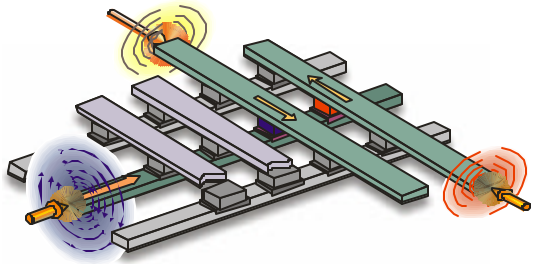






**New (smaller, cheaper, faster) devices**

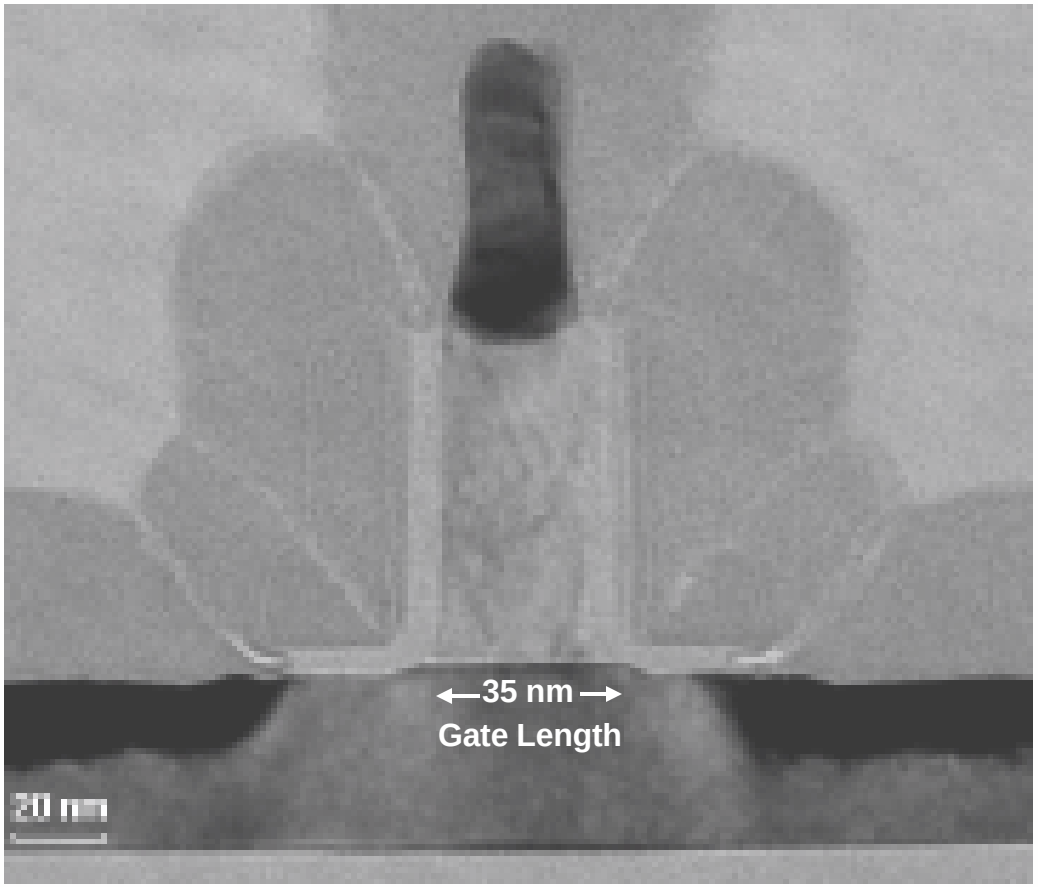


# Topics

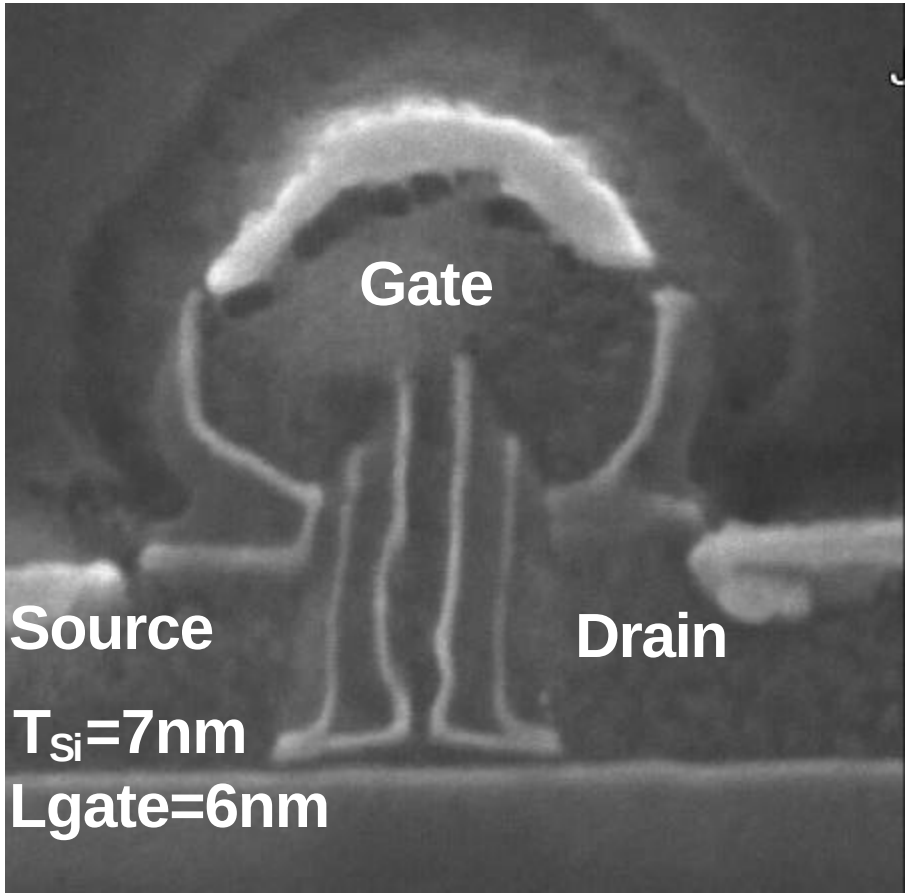
- The extension of silicon CMOS technology
- The search for the “ultimate” FET
- “Beyond the FET”:
  the Nanoelectronics Research Initiative
- A Personal Outlook:
  prospects for adiabatic switching and reversible logic

# The silicon transistor in manufacturing …



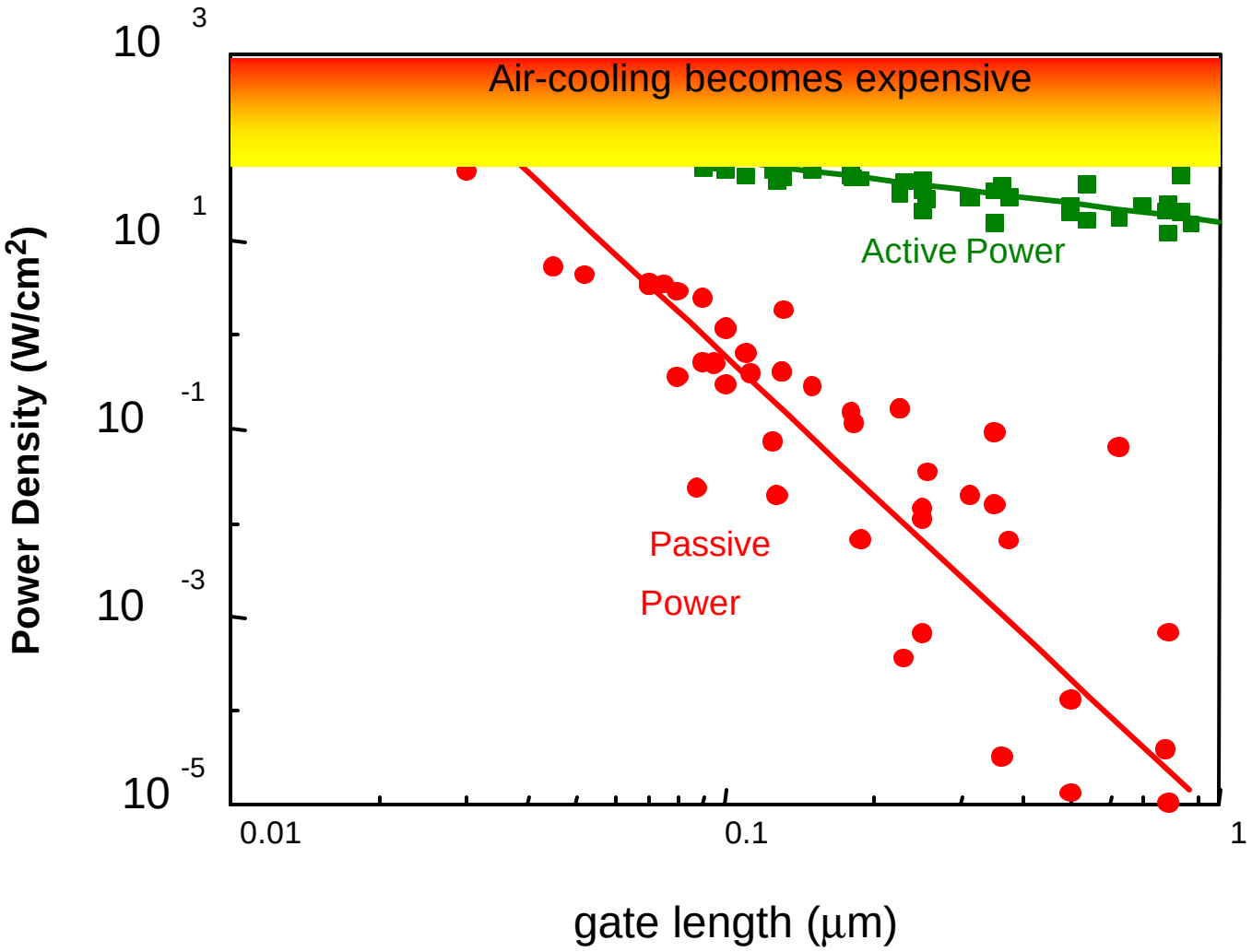

**90 nm technology generation**

# … and in the lab.

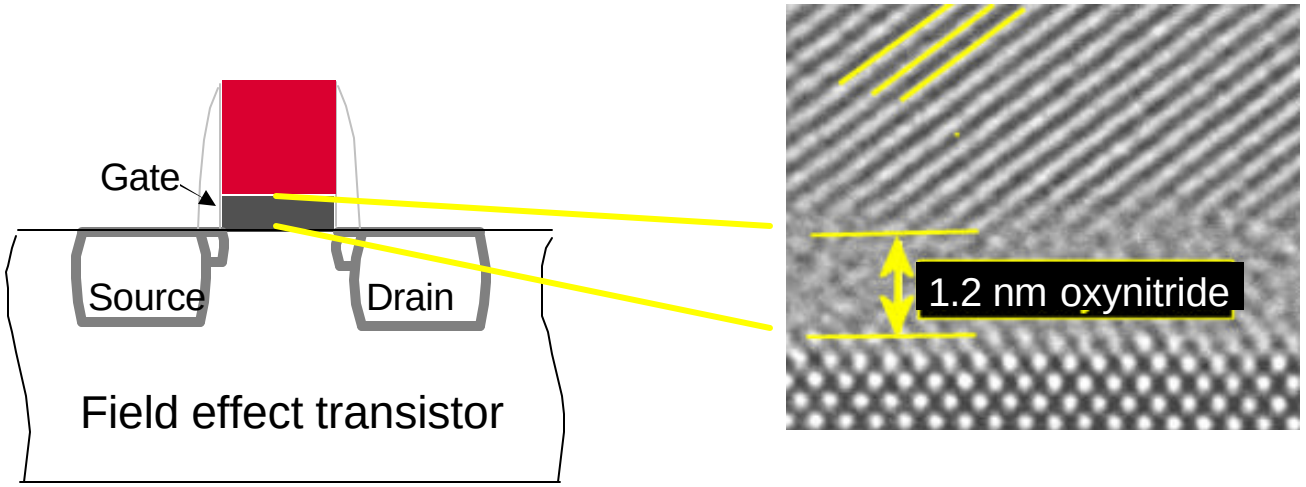



**B. Doris et al., *IEDM* , 2002**

# Still, we are approaching some limits.

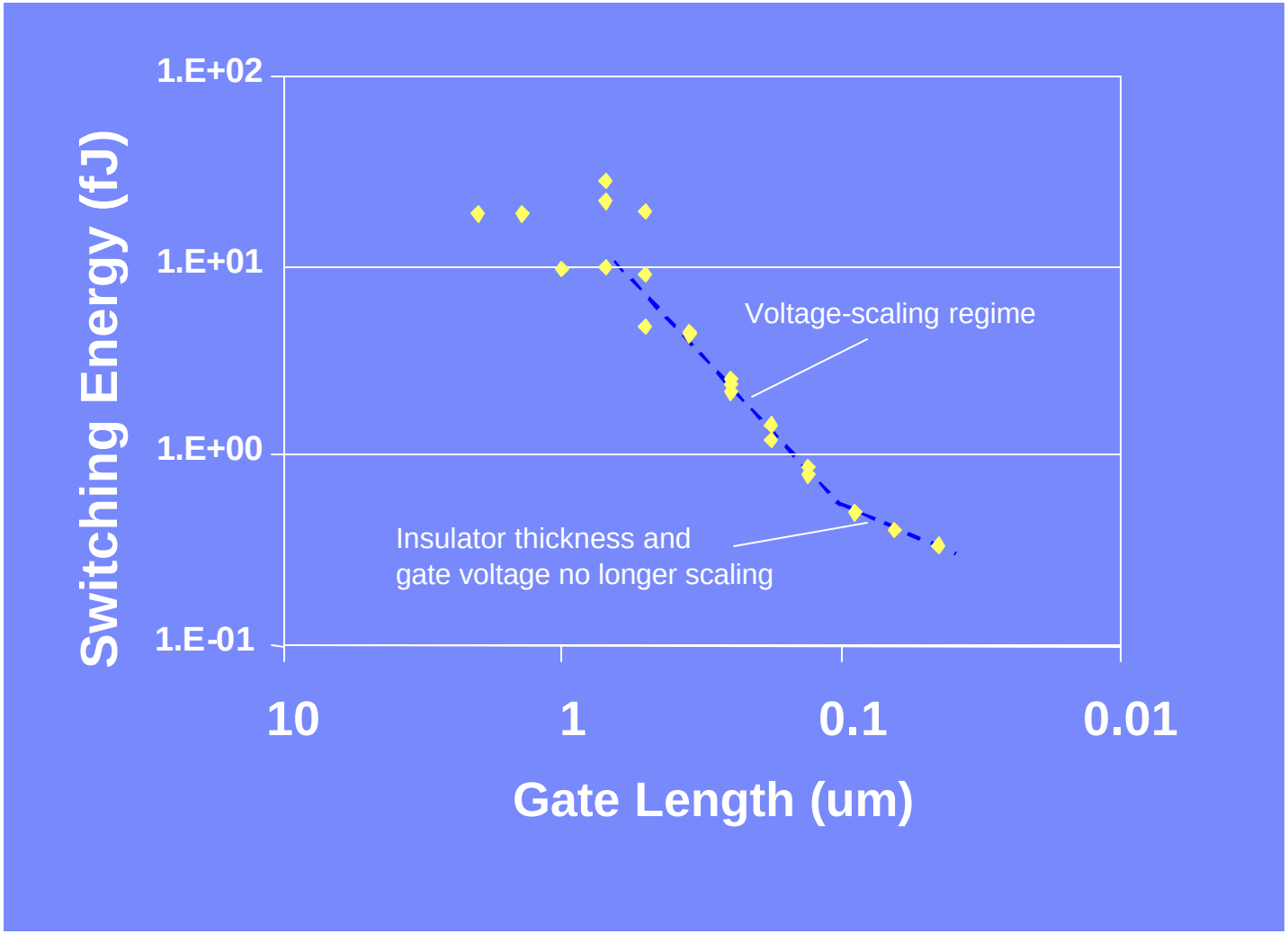


# The Problem with Passive Power Dissipation: The Inability to Scale Atoms

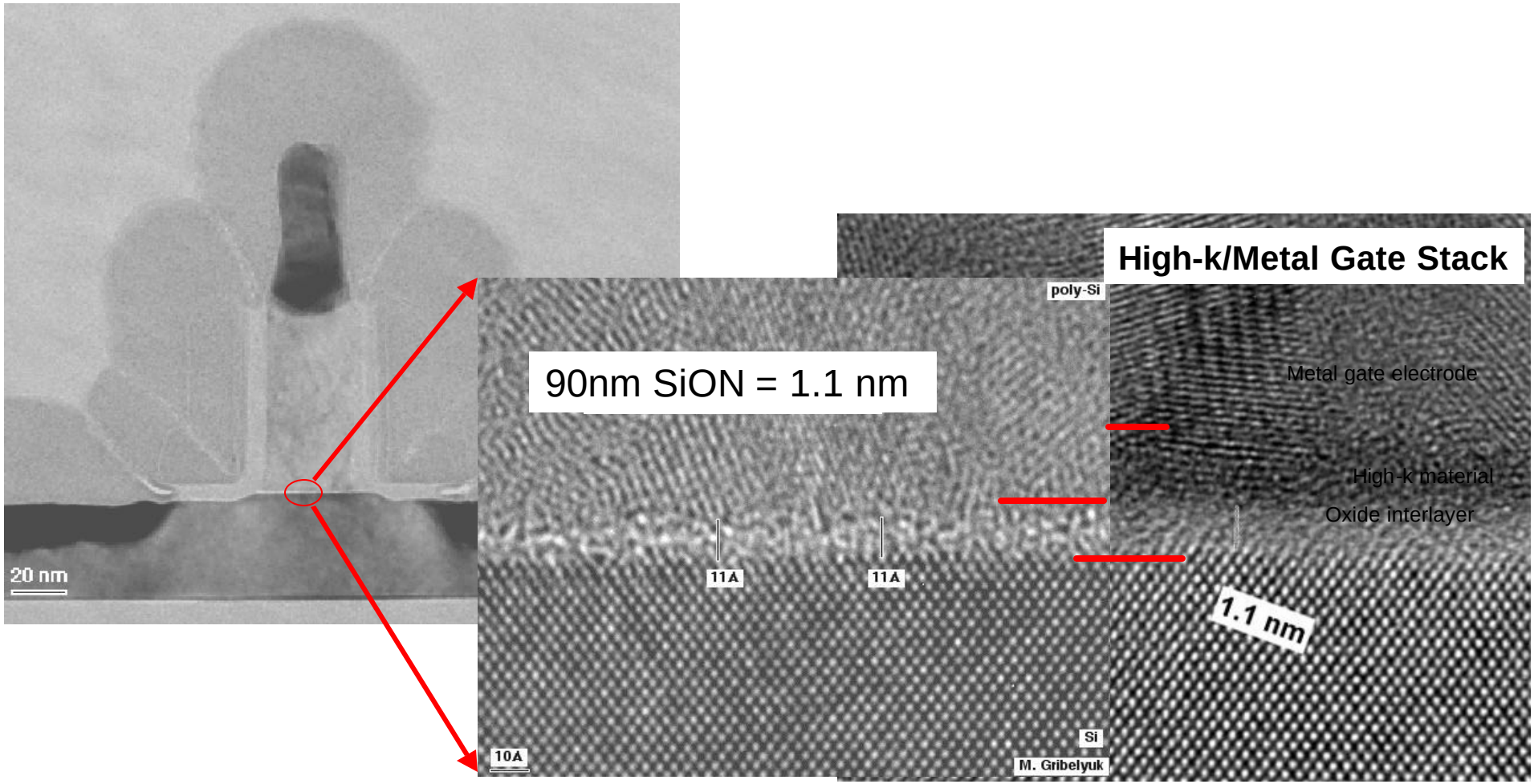



- Direct tunneling through the gate insulator will be the dominant cause of static power dissipation.
- Single atom defects can cause local leakage currents 10 – 100x higher than the average current, impacting reliability and generating unwanted variation between devices.

# Switching energy is declining at a slower rate.



# The Work-Around: High-k Insulator / Metal Gate Stack



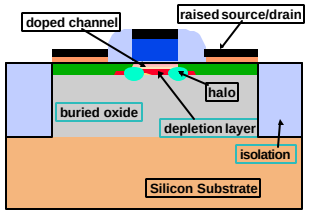

**90nm Gate Dielectric:**
**Tinv = 19A**
**ToxGL = 11A**

**High-k/Metal Gate Stack:**
**Tinv = 14.5A**
**ToxGL = 16A**

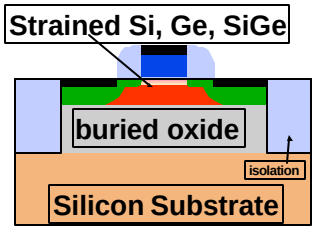
# Innovation Will Continue: Transistor Roadmap Options

| | 2004 | 2007 | 2010 | 2013 | 2016 | 2020 |
|---|---|---|---|---|---|---|
| **Physical Gate** | 37 nm | 25 nm | 18 nm | 13 nm | 9 nm | 6 nm |

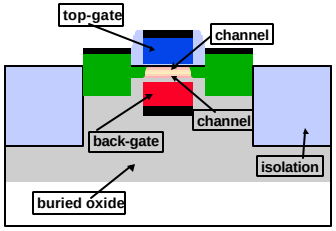
**Ultrathin SOI**



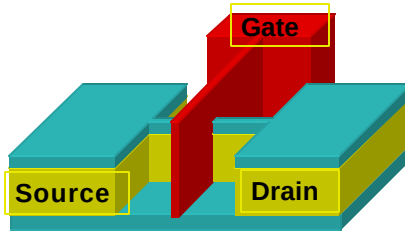

**High *k* gate dielectric**




**Double-Gate CMOS**

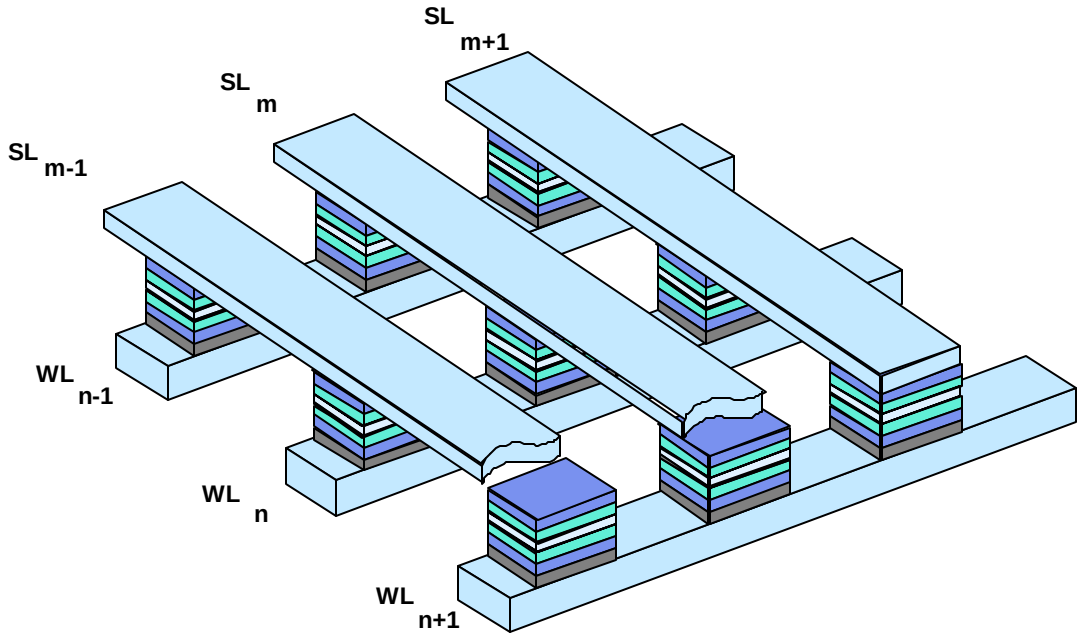



**FinFET**




In general, growing power dissipation and increasing process variability will be addressed by introduction of new materials and device structures, and by design innovations in circuits and system architecture.

# Memory may be easier to shrink than logic.



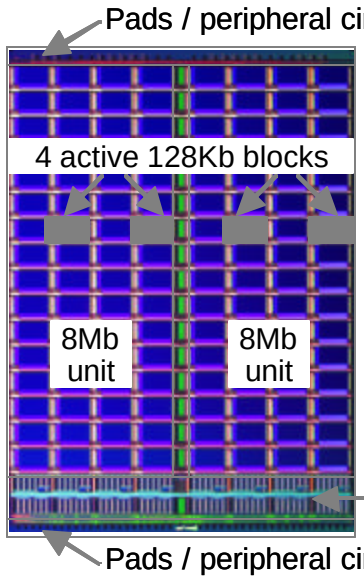

- Everyone is looking for a dense (cheap) cross-point memory.
- It is relatively easy to identify materials that show bistable hysteretic behavior (easily distinguishable, stable on/off states).

# Some Classes of Novel Memory Devices Under Development by Commercial Entities

- Extensions of Silicon Nonvolatile (Flash) Memory
- Magnetic Tunnel Junctions (MRAM)
- Chalcogenide Phase Change Materials (PCM)
- Ferroelectric Polymers
- Hysteretic Conduction in Complex Metal Oxides
- Solid-State Electrochemical Systems
- (Nano) Electro-Mechanical Systems
- and more …

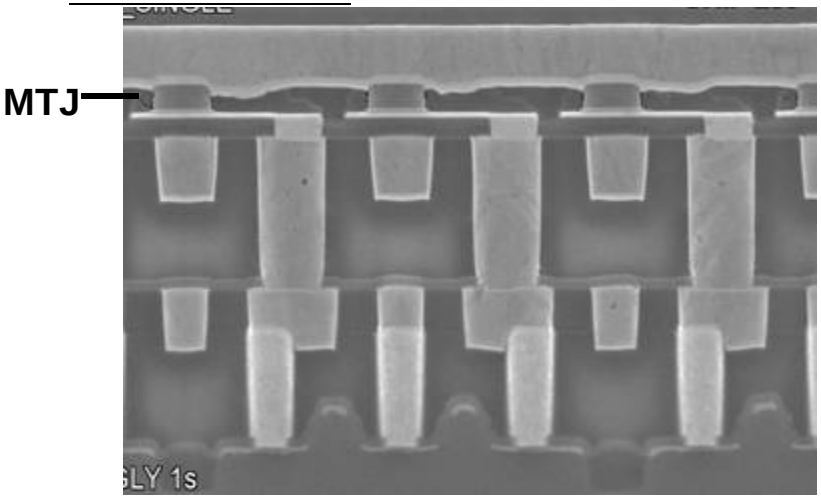
# Example: 16Mbit IBM MRAM Demonstration

**Chip image:**



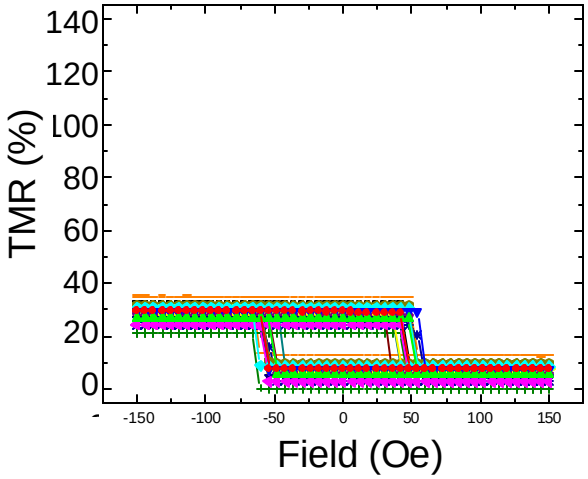

- 4 active bits / block
- Good power supply distribution
- Write currents trimmed by block

**Cross-section:**

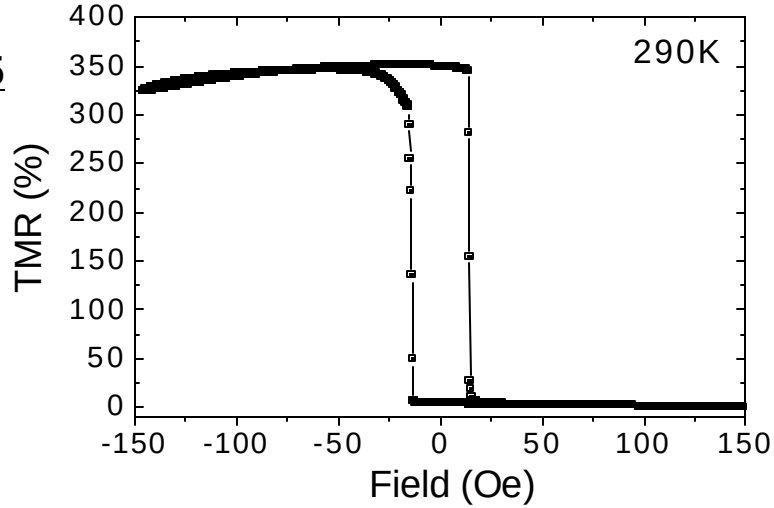



## Materials Advances

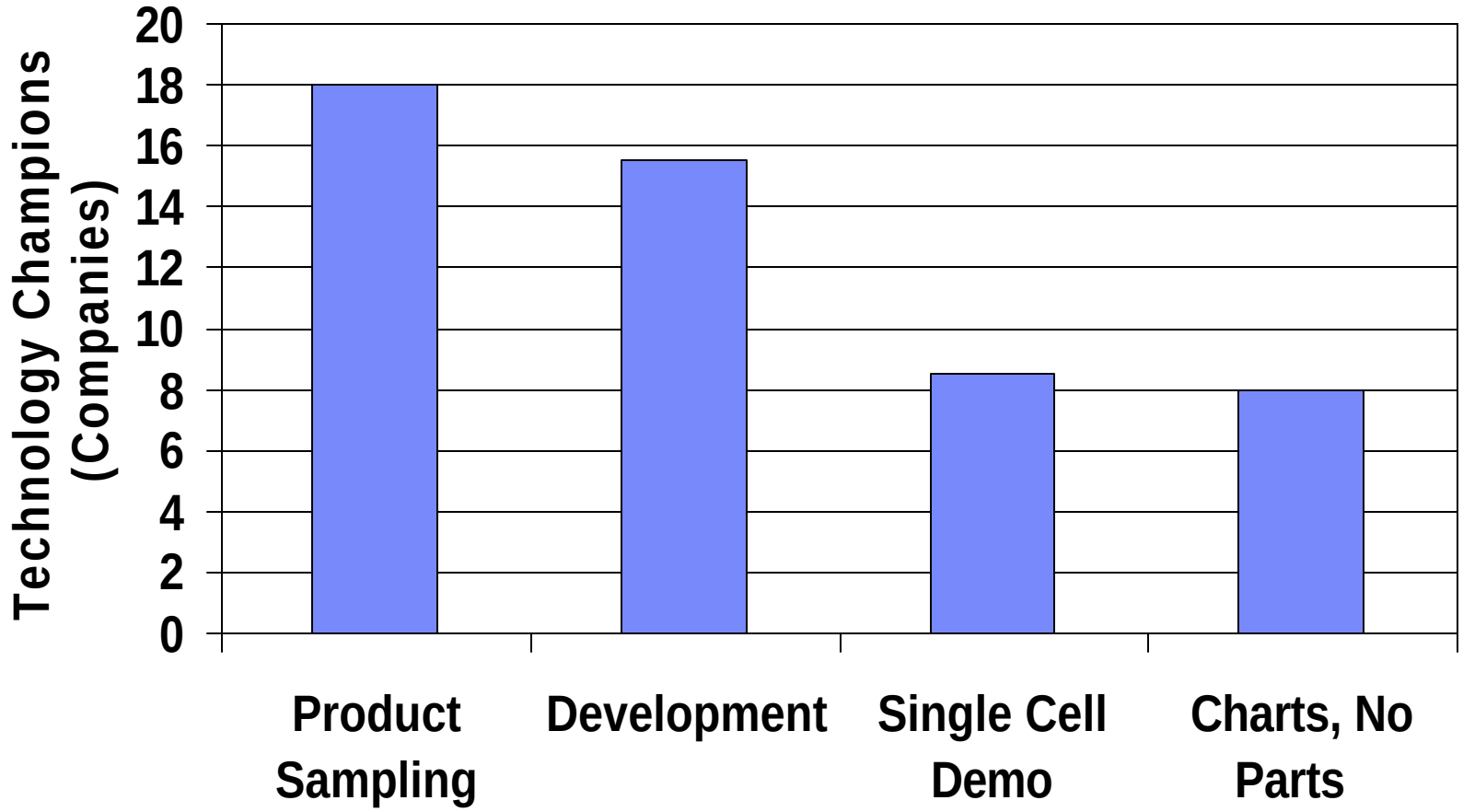
**1995**



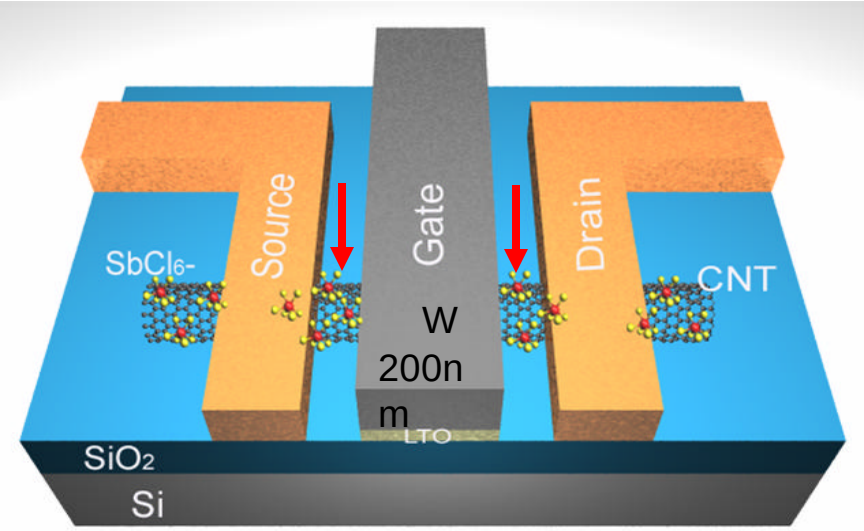

**2005**



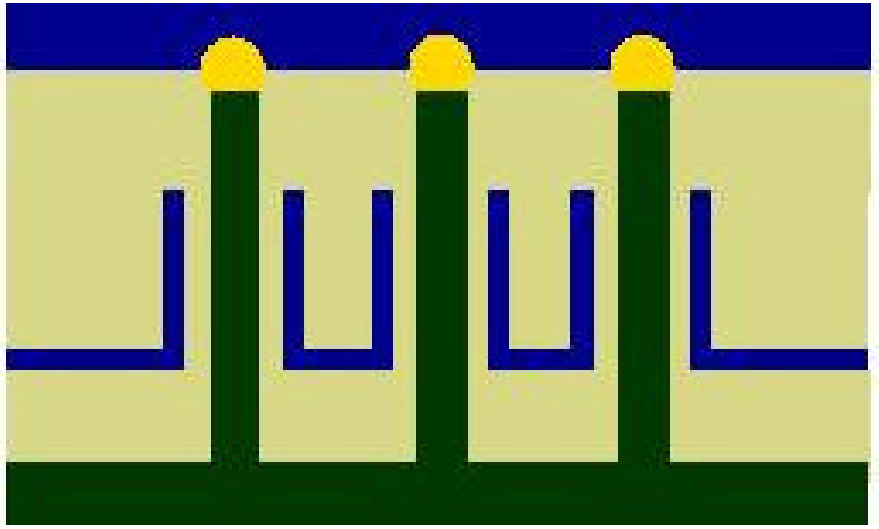
# Relative Maturity of Nonvolatile Memory Technologies (2005)



# Post-Silicon CMOS: The Quest for the Ultimate FET

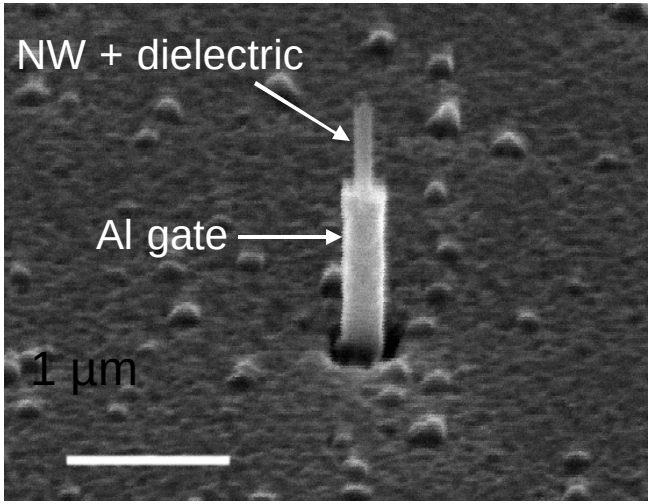


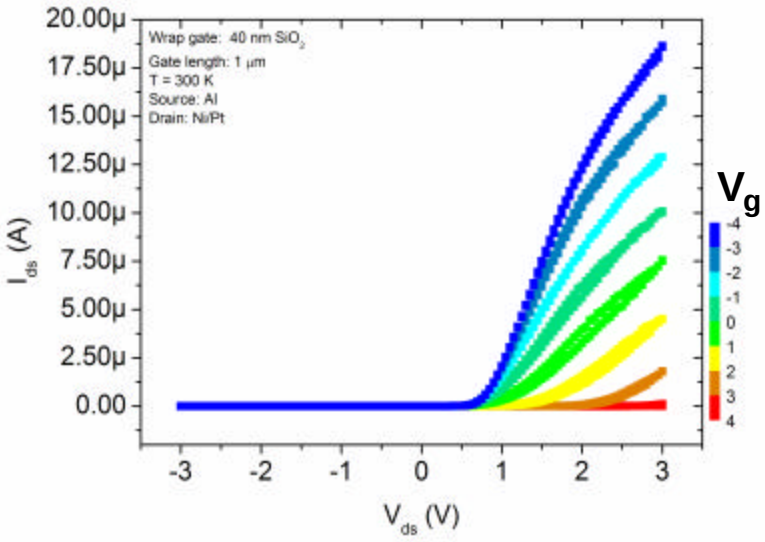

Self-Aligned Carbon Nanotube FET:
Extension Contacts Based on
Charge-Transfer Chemical Doping

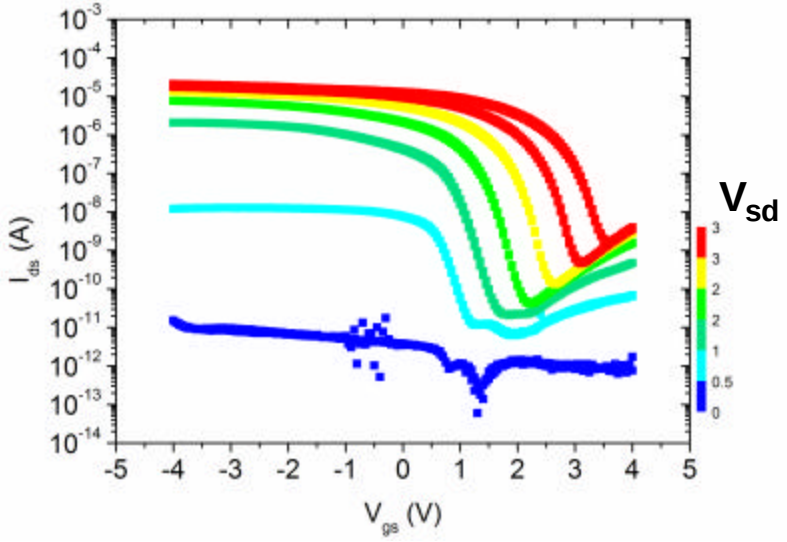


Vertical Transistor
Based on Semiconductor Nanowires

# Vertical Silicon Nanowire FET

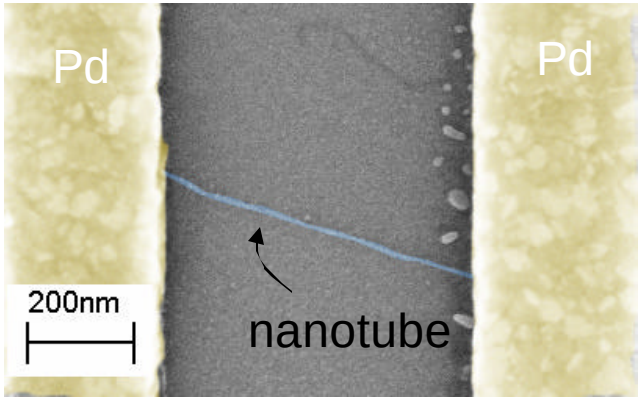


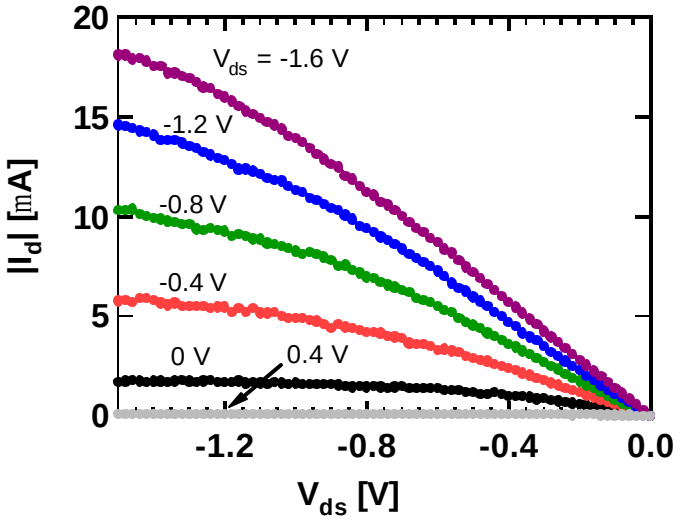



# Intrinsic Performance of Cabon Nanotube FETs

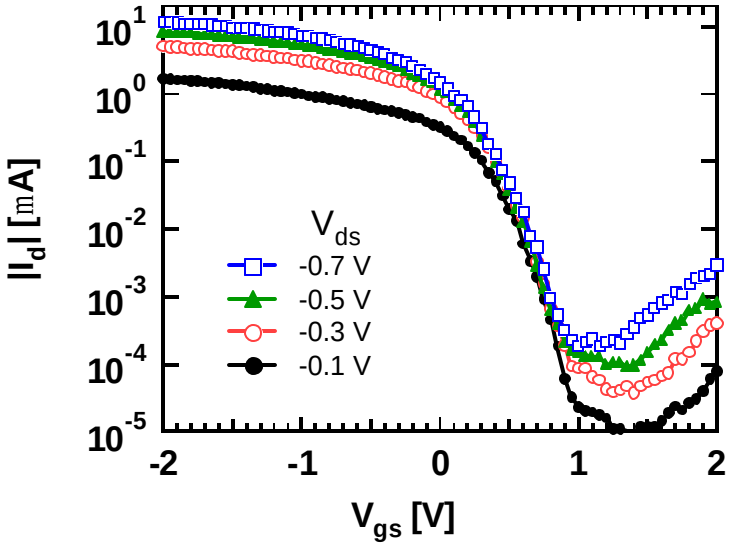
Simple back-gated CNTFET



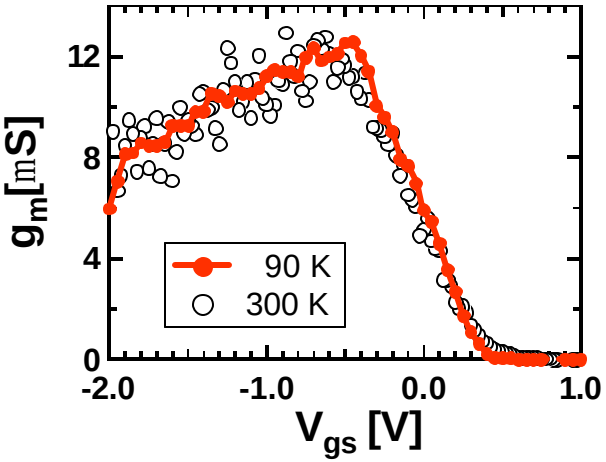

Output Characteristics




Subthreshold Characteristics




Temperature dependence




Yu-Ming Lin *et al.* (IBM), EDL 2005

# Intrinsic Switching Speed of CNFETs

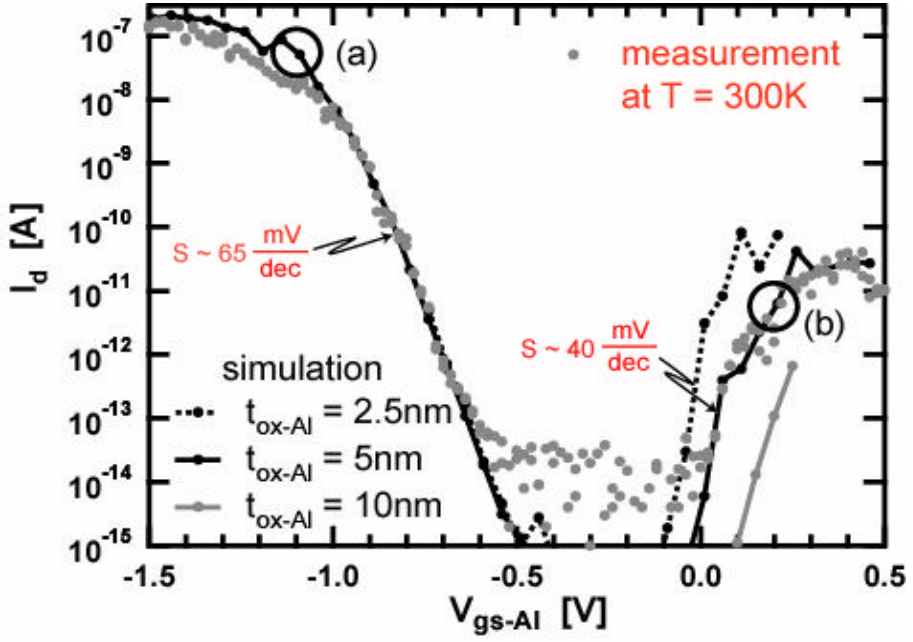
Cut-off Frequency $f_T = \frac{g_m}{2p\,C_g}$ $C_g$ : gate capacitance

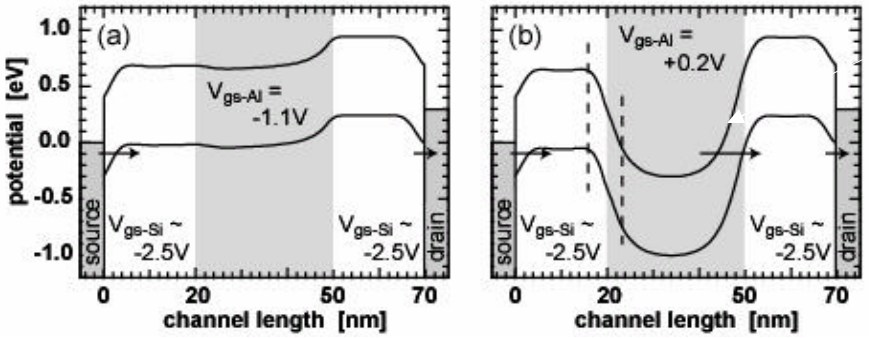
| | **Lin et al. (IBM)** | **Javey et al. (Stanford)** | **Seidel et al. (Infineon)** |
|---|---|---|---|
| Diameter | ~ 1.8 nm | ~ 1.7 nm | ~ 1.1 nm |
| Gate Dielectric | 10-nm $SiO_2$ | 8-nm $HfO_2$ | 12-nm $SiO_2$ |
| Maximum $g_m$ | 12.5 µS | 27 µS | 3.5 µS |
| $C_g/L$ | 38 pF/m | 120 pF/m | 32 pF/m |
| $f_T$ @ $L_g$ = 65 nm | **800 GHz** | 550 GHz | 260 GHz |

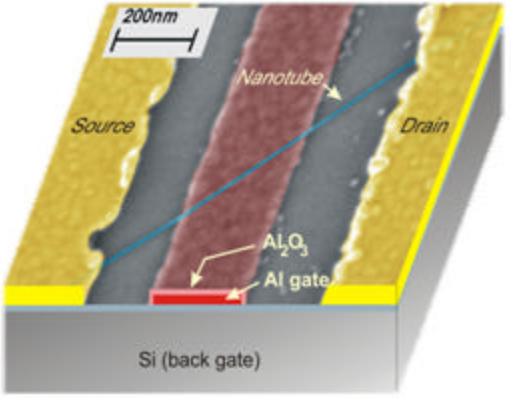
Yu-Ming Lin *et al.* (IBM), EDL 2005

# Carbon Nanotube FET:

## Potential for greatly improved turn-on characteristics (low-voltage operation)




Dual-Gate
CNTFET

J. Appenzeller, Y.-M. Lin,
J. Knoch, and Ph. Avouris,
Phys. Rev. Lett. **93**, 196805 (2004)

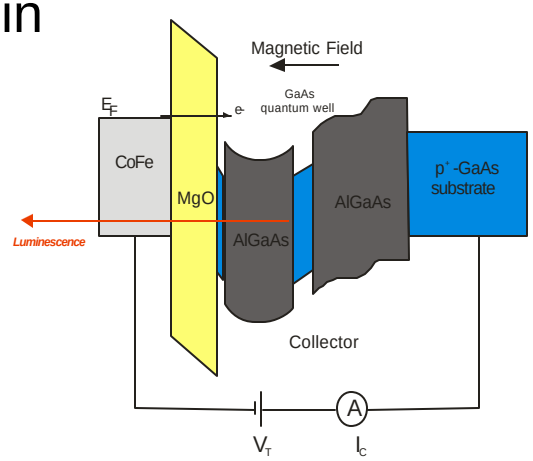
# Will there be a successor to the FET?

- Many have written about this subject.
- An article by George Bourianoff (“The Future of Nanocomputing”, IEEE Computer 36, pp. 44–53) sparked discussions within the Semiconductor Research Corporation regarding the objectives of a new research program – the Nanoelectronics Research Initiative (NRI) – which would stimulate the exploration of devices “beyond the FET”.

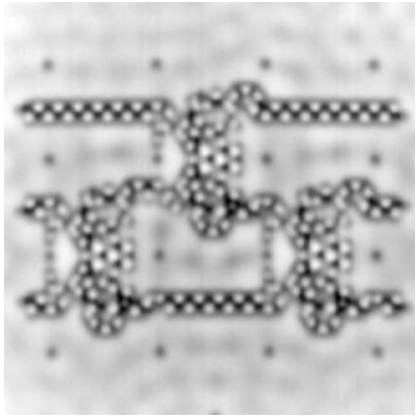
→ computational state vectors other than electronic charge

# Beyond Charged-Based Logic?

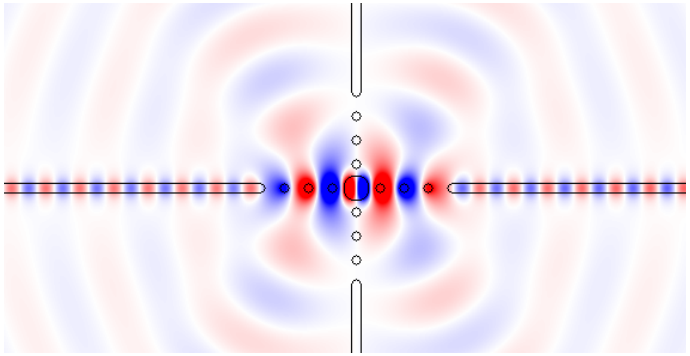
- Spin




- Nanomechanics



- Photons and Plasmons



- Biochemistry

# Nanoelectronics Research Initiative (NRI)

- AMD, Freescale, Micron, TI, IBM, Intel
  → Joint Industry funding of University Research
- Promoting both
  - Invention / Discovery (distributed research, “let many flowers bloom”)
  - Proof of Concept (focused university consortia with outstanding facilities)
- “Extend the historical cost/function reduction, along with increased performance and density … orders of magnitude beyond the limits of CMOS”
  - Computational State Vectors other than Electronic Charge
  - Non-equilibrium Systems
  - Novel Energy Transfer Mechanisms
  - Nanoscale Thermal Management
  - Directed Self-assembly of such structures

# Nanoelectronics Research Initiative (NRI):

## Announced Dec. 8, 2005, at *Silicon Nanoelectronics and Beyond, by NSF and SRC*

- Institute for Nanolectronics Discovery and Exploration (INDEX)
  - Lead Institution: College of Nanoscale Science and Engineering at the University of Albany (SUNY)
  - MIT, Georgia Institute of Technology, Harvard, RPI, Yale, Purdue
  - Spintronic and molecular configurational switches
- Western Institute of Nanoelectronics (WIN)
  - Lead Institution: UCLA Henry Samueli School of Engineering and Applied Science
  - UCLA, UC Berkeley, UC Santa Barabara, Stanford
  - Spintronic and plasmonic devices
- Southwestern Academy of Nanoelectronics (SWAN)
  - Lead Institution: UT Austin Microelectronics Research Center
  - Texas A&M, UT Dallas, ASU, Notre Dame, U. of Maryland, Rice U.
- Supplemental NSF/NRI grants to existing NSF centers

# NSF/NRI Supplemental Awards: 2005

| PI | Institution | Center | Center Name | Title of Supplement |
|---|---|---|---|---|
| Lundstrom, Mark | Purdue U | NCN | Network for Computational Nanotechnology | Exploratory Theory, Modeling, and Simulation for the NRI |
| Yardley, James T. | Columbia U | NSEC | Columbia Center for Electronic Transport in Molecular nanostructures | Non-equilibrium Quantum Coherent Devices in 1-D materials |
| Westervelt, Robert | Harvard U | NSEC | Science of Nanoscale Systems and their Device Applications | Ultrasmall Nanowire and Oxide Switches |
| Hawker, Craig | UCSB (Stanford, U Mass) | MRSEC | MRSEC at UCSB | Development of Next Generation Devices using Nanolithographic Techniques |
| Hull, Robert | U Virginia (Notre Dame) | MRSEC | Center for Nanoscopic Materials | Directed Assembly of Epitaxial Semiconductor Nanostructures for Novel Logic Switches |
| Johnson, Matt | U. Arkansas/ U Oklahoma | MRSEC | Center for Semiconductor Physics in Nanostructures | Nanoferroelectric Random Access Memory |

NSF issued new RFP on 8/18/06 for new set of awards

# WIN Organizational Structure

**Director: Kang Wang**

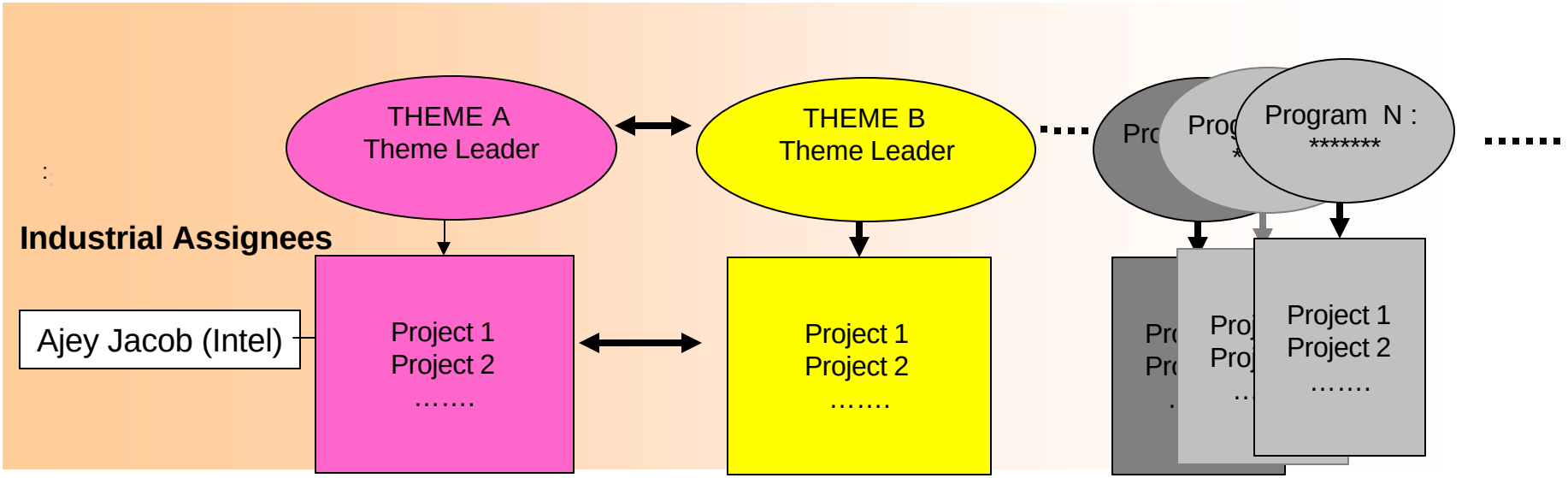
**Chief Operating Officer**
Kos Galatsis

**Admin**
Cost Shared CNSI
(Katie Christensen)

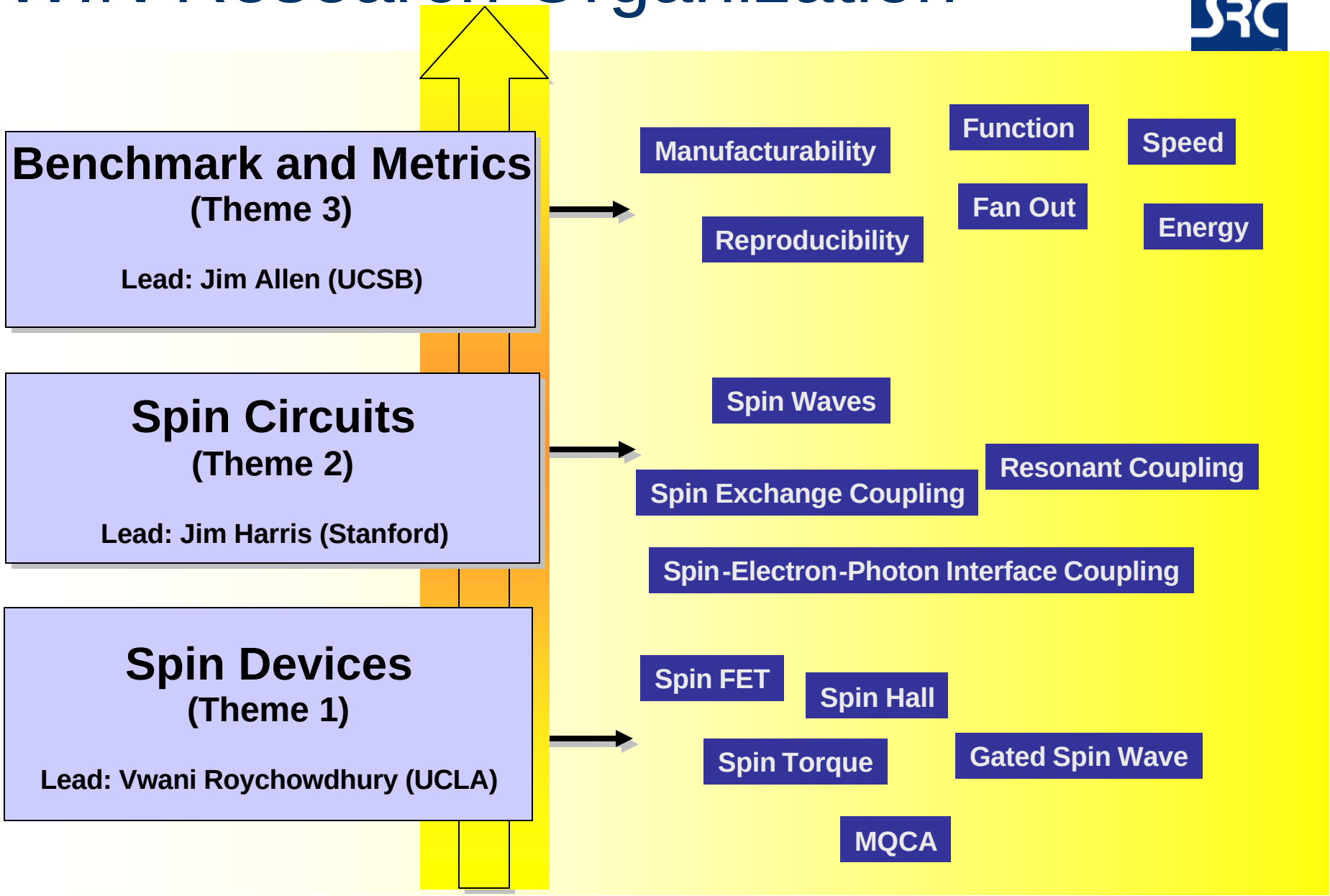
**Equipment & Facilities**
Cost Shared CNSI

**Industrial Program Manager: Youssry Botros (Intel)**

**Executive Committee:**
- **Kang Wang (UCLA)**
- **David Awschalom (UCSB)**
- **Jeff Bokor (UC Berkeley)**
- **James Harris (Philip Wong) (Stanford)**
- **4 Industrial reps:**
  - **George Bourianoff**
  - **Jeff Welser**
  - **Sandhu S. Gurtej**
  - **Ming-Ren Lin**



# WIN Research Organization



# INDEX Details

- Structure
  - Headquartered at UAlbany-CNSE
  - 7 university partners: UA, MIT, GIT, Harvard, Purdue, RPI, Yale
  - Lead PIs: A. Kaloyeros, D. Antoniadis, and J. Meindl
  - Work divided into 5 tasks
    - *Task I: Novel computing State Variable Devices*
    - *Task II: Fabrication and Self-assembly*
    - *Task III: Modeling and Architecture*
    - *Task IV: Theory and Simulation*
    - *Task V: Strategy and Roadmap*

- Timeline
  - Year 1: Emphasis on Tasks I & II
  - Year 2: Add Task III
  - Year 3: Add Tasks IV & V

- Management
  - Leadership Council with academic and industrial representatives
  - Technical advisory group from industry

# INDEX Technical Program and Funding

- Research Areas
  - ***Task I: Novel computing State Variable Devices***
    - ***Magnetoresistive devices using magnetic flux quantum as state variable***
    - ***Spintronic single electron tansistors based on the Rashba Effect***
    - ***Non-volatile logical switches based on the giant planar Hall Effect***
    - ***Molecular-mechanical relays using voltage dependent ion channels***
    - ***Graphene nanowire switches***
    - ***Metal-arene based molecular conformational switches***
  - ***Task II: Fabrication and Self-assembly***
    - ***Focus for the first 3 years is on fabrication techniques for the Task I devices***
    - ***This task is responsible for coordination between the facilities***
  - ***Task III: Modeling and Architecture***

# SWAN Team

- **Coordinator / Lead PI: Sanjay Banerjee (UT-Austin)**

- **University of Texas (Austin)**
  - **Alan MacDonald, Mathew Gilbert, Frank Register**
- **University of Texas at Dallas**
  - **Bruce Gnade, Moon Kim**
- **Texas A& M University**
  - **Jairo Sinova**
- **Rice University**
  - **Yehia Massoud, Peter Nordlander, Naomi Halas**
- **University of Maryland**
  - **Sankar DasSarma**
- **Notre Dame**
  - **Wolfgang Porod and Gary Bernstein**
- **Arizona State University**
  - **John Shumway**

- Plan to establish additional relationships with Oak Ridge National Labs, NASA JSC, and potentially other schools / national labs

# SWAN Tasks and Investigators

- **LEAD PI: Prof. Sanjay Banerjee, UT-Austin**
- **Task 1: Logic Devices based on new computational state variables**
  - **UT: Banerjee, Gilbert, MacDonald, Register; Maryland: DasSarma, TAMU: Sinova, ASU: Shumway**
- **Task 2: Novel materials and structures**
  - **TAMU: Sinova; Notre Dame: Porod, , Bernstein; UT: Gilbert, Banerjee, Maryland: DasSarma**
- **Task 3: Directed Self-assembly and nanoscale thermal management**
  - **UT: Gilbert, Register, Banerjee; Maryland: DasSarma**
- **Task 4: Novel interconnect and architectures**
  - **Rice: Massoud, Nordlander, Halas**
- **Task 5: Nanoscale Characterization**
  - **UT Dallas: Gnade/Kim**

# Conclusions

- Silicon CMOS logic will be extended at least another 10 years.
  - New materials and transistor structures
  - Cooperative circuit and device technology co-design
- New non-silicon memory devices are poised to enter the market.
- The “ultimate FET” may not contain silicon.
- NRI will promote the search for logic devices “beyond the FET”.
- Prediction: Research looking “beyond the FET” will converge on
  - Energy-conserving dynamical systems best suited for implementation of adiabatic switching and reversible logic.
  - Novel circuit architectures designed to allow reliable computation with unreliable devices.