



**MARK PINTO, PH.D.**

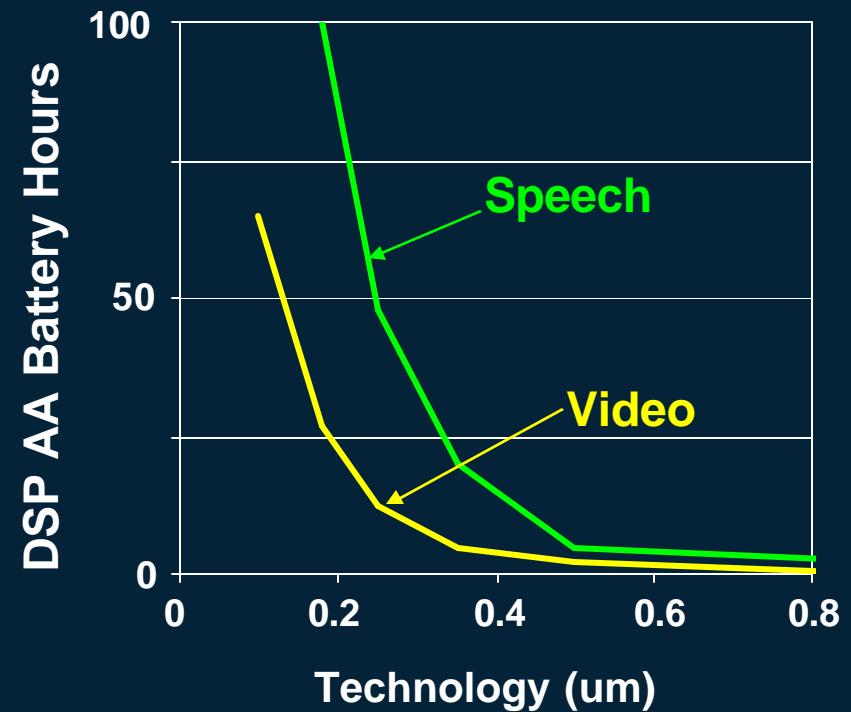
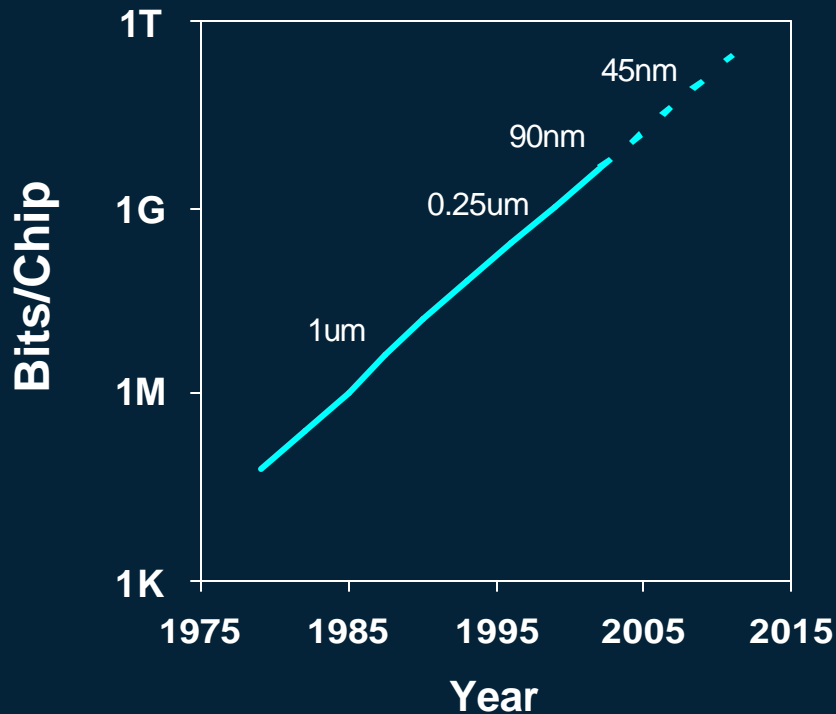
# NANOMANUFACTURING TECHNOLOGY

NAS/SSSC Spring Meeting  
April 2, 2009

APPLIED MATERIALS.

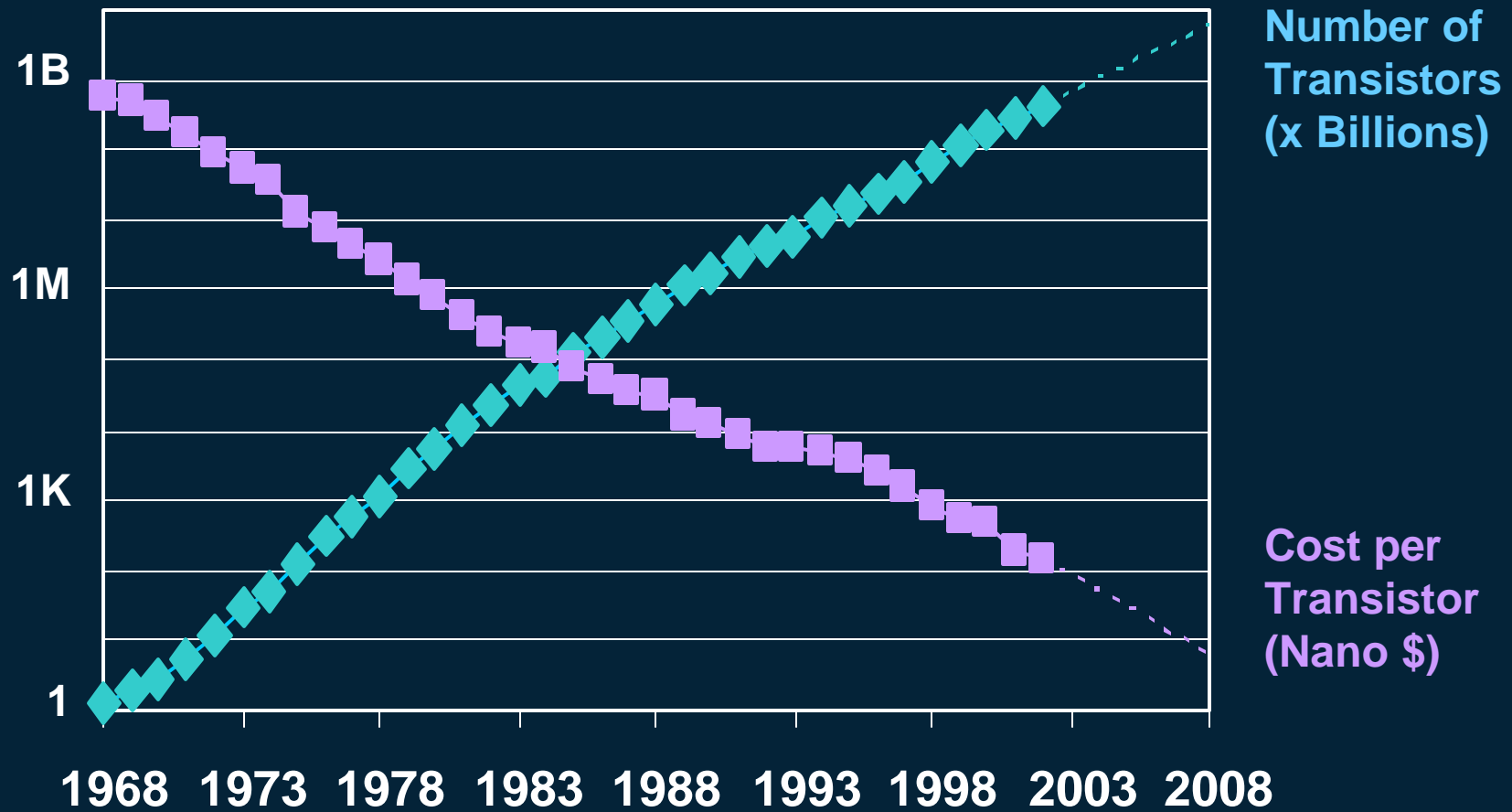
EXTERNAL USE

# Moore's Law and Transistor Scaling



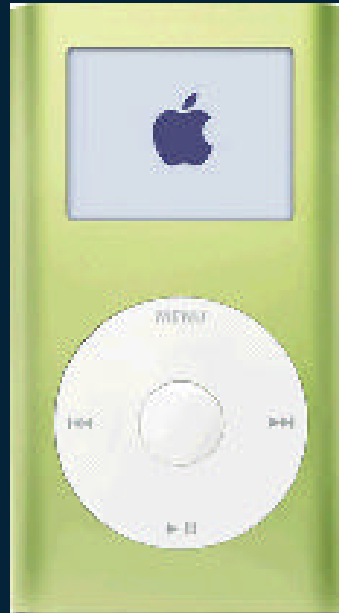
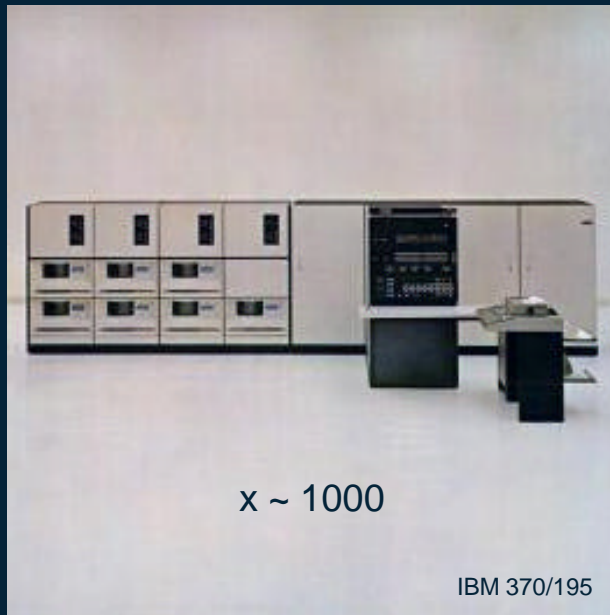
- Decrease transistor dimensions by  $k$ , drop voltage by  $k$
- Circuit area reduced by  $1/k^2$ , speed increased by  $k$
- Power per circuit reduced by  $1/k^2$ , power per area constant

# Moore's Law and Transistor Cost



(Source: G. Moore, ISSCC 2003)

# A Recent Product Enabled by Nanoelectronics



**1975 = \$1B<sup>†</sup>**

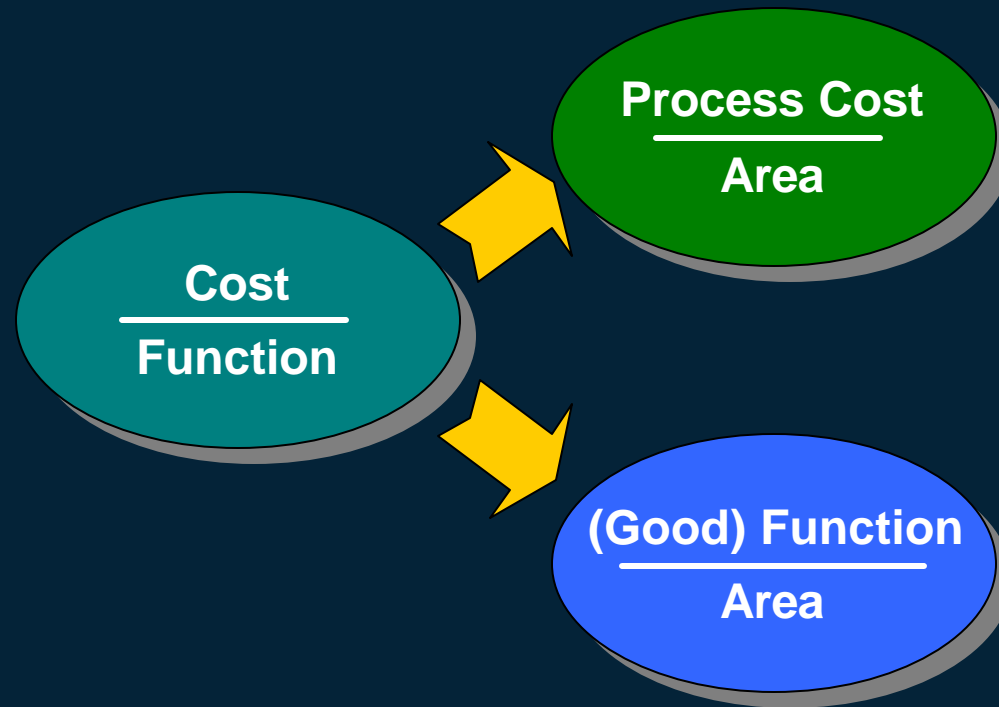
**2006 ~ \$200**

**2020 = 5¢<sup>\*</sup>**

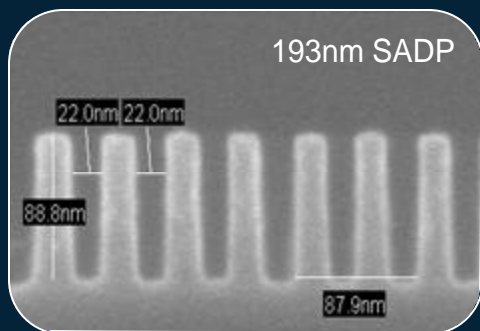
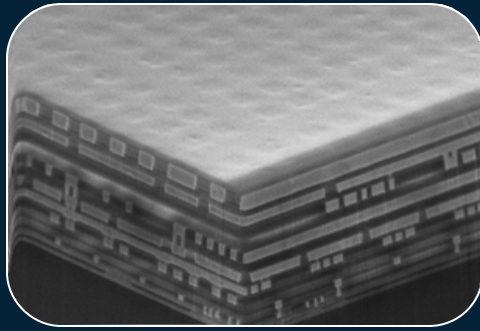
† Memory cost only

\* Extrapolating memory cost reduction factor over last 30 years and display cost/area over last 10 years

# Cost Per Function



# Cost Per Function: VLSI Technology



Cost  
Function

Process Cost  
Area

(Good) Function  
Area

Scaling has been the primary cost driver for ICs – but not at an overcompensating increase in process cost/area



# Patterning Is More Than Printing

## PRODUCTIVITY

- Automation
- eDiagnostics
- Material Handling
- Reticle Management

## PREPARATION

### Patterning Films

- CVD Hardmask
- CVD ARC/Spin-on ARC
- PVD Hardmask

### Planarity Enhancement

- Ecmp
- Real-Time Profile Ctrl
- Fixed-Abrasive CMP

## PRINTING

- Scanner
- Track
- Mask/Mask Etch
- Photoresist
- $K_1$  reduction

## PATTERN TRANSFER

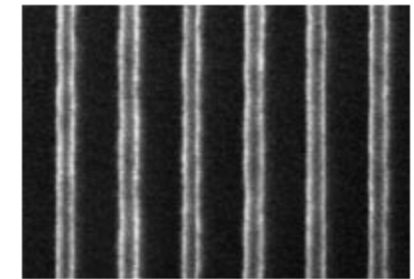
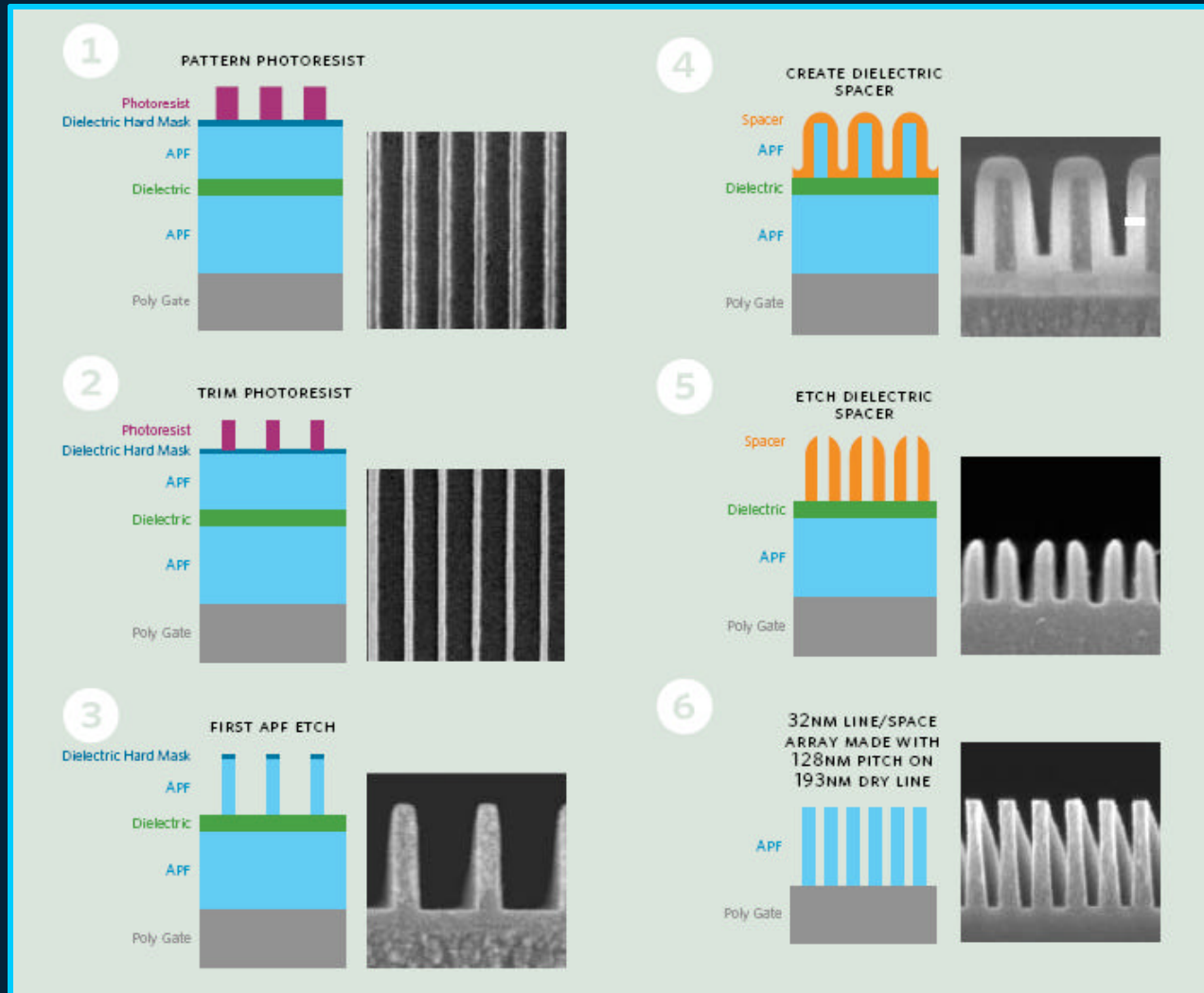
### Etch

- High Aspect Ratio Etch
- Critical Etch
- Damascene Etch
- Trimming

## PROCESS CONTROL/DFM

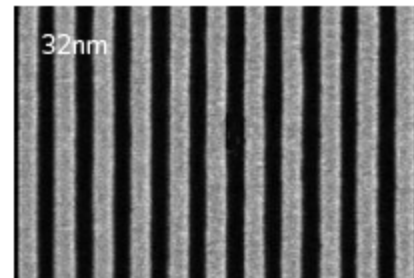
- CD SEM
- OPC Qualification
- APC
- Defect Inspection and Review
- Overlay

# Self Aligned Double Patterning



after lithography

LER = 3.1nm (3 $\sigma$ )



after final APF etch

LER = 1.5nm (3 $\sigma$ )



# Progress Through Materials Innovation

1 H 1.0079																
3 Li 6.941	4 Be 9.0122															
11 Na 22.990	12 Mg 24.305															
19 K 39.098	20 Ca 40.078	21 Sc 44.956	22 Ti 47.867	23 V 50.94												
37 Rb 85.468	38 Sr 87.62	39 Y 88.906	40 Zr 91.224	41 Nb 92.906												
55 Cs 132.91	56 Ba 137.33	57-71 *	72 Hf 178.49	73 Ta 180.95												
87 Fr (223)	88 Ra (226)	89-103 Ac														
			57 La 138.91	58 Ce 140.12												
			89 Ac (227)	90 Th 232.04												

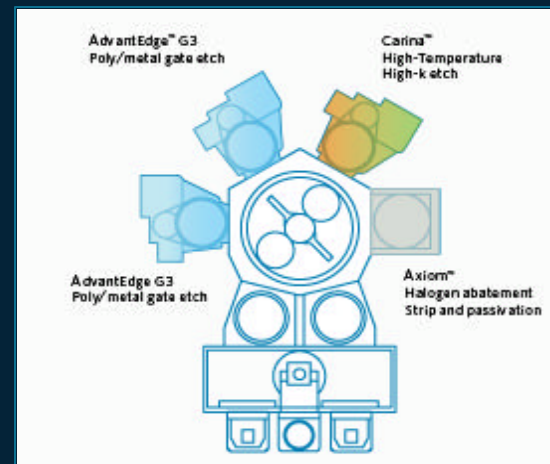
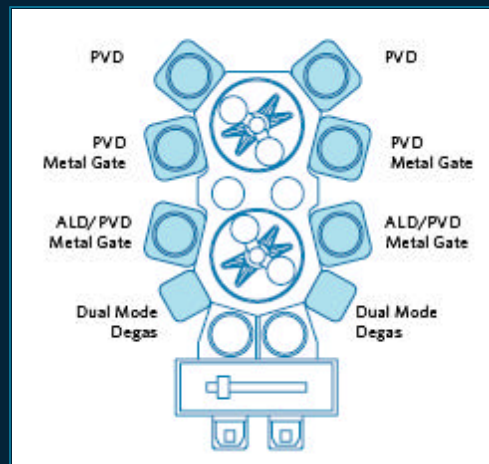
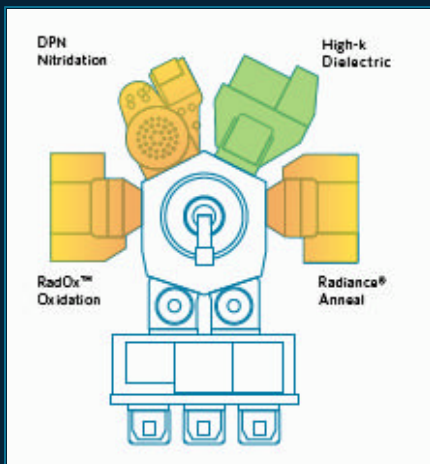
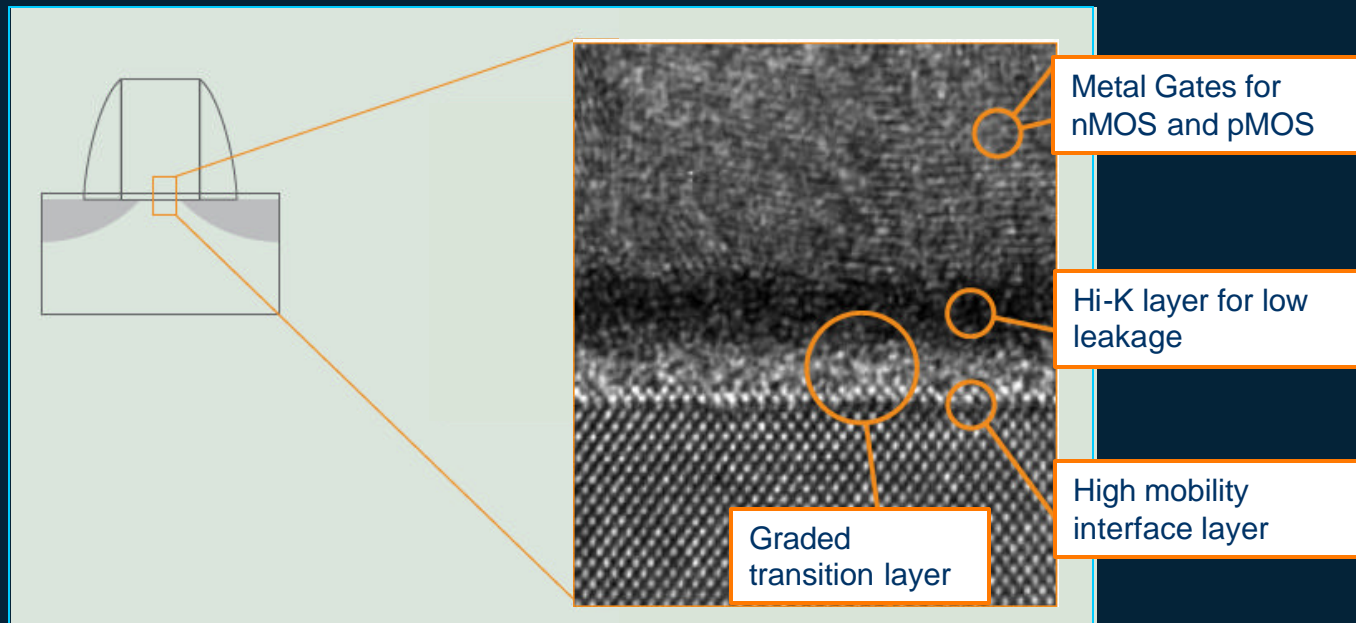
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37 Rb 85.468	38 Sr 87.62	39 Y 88.906	40 Zr 91.224	41 Nb 92.906	42 Mo 95.94	43 Tc (98)	44 Ru 101.07	45 Rh 102.905	46 Pd 106.36	47 Ag 107.868	48 Cd 112.411	49 In 114.818	50 Sn 118.710	51 Sb 121.757	52 Te 127.6	53 I 126.905	54 Xe 131.29	55 Ba 137.33	56 La 138.905	57 Ce 140.12	58 Pr 140.907	59 Nd 144.24	60 Pm (144.912)	61 Sm 150.36	62 Eu 151.964	63 Gd 157.25	64 Tb 158.925	65 Dy 162.50	66 Ho 164.930	67 Er 167.259	68 Tm 168.930	69 Yb 173.054	70 Lu 174.967

[2000s]

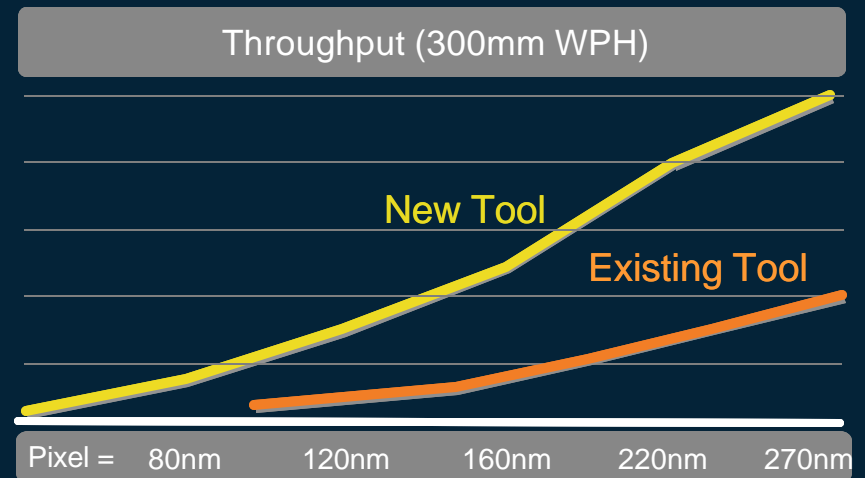
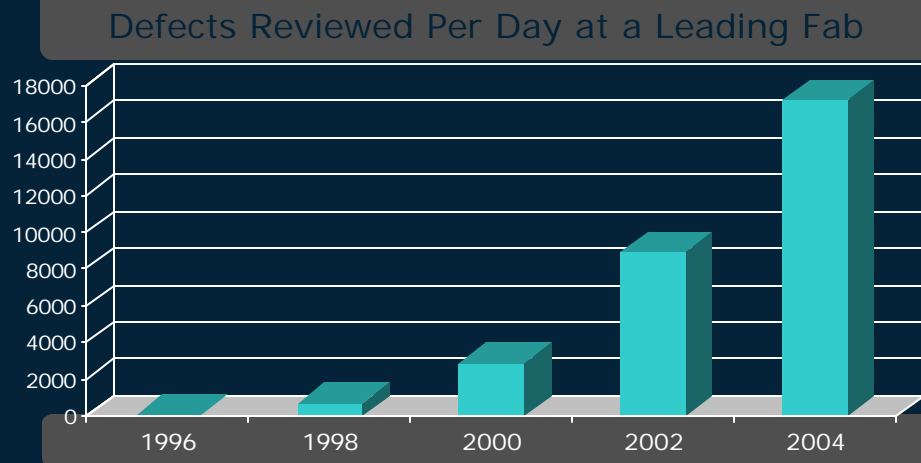
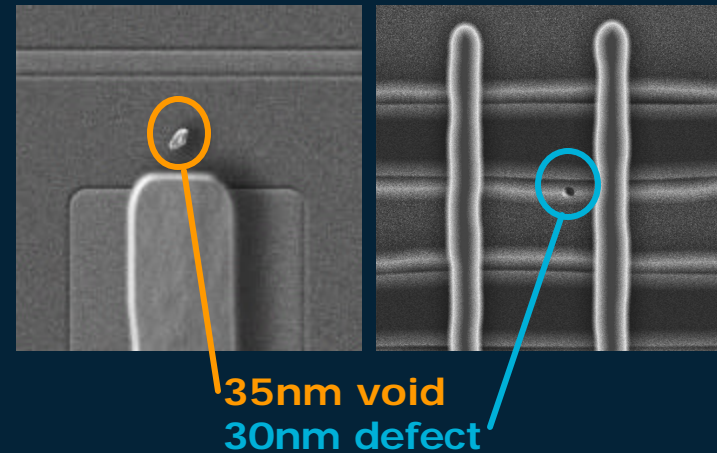
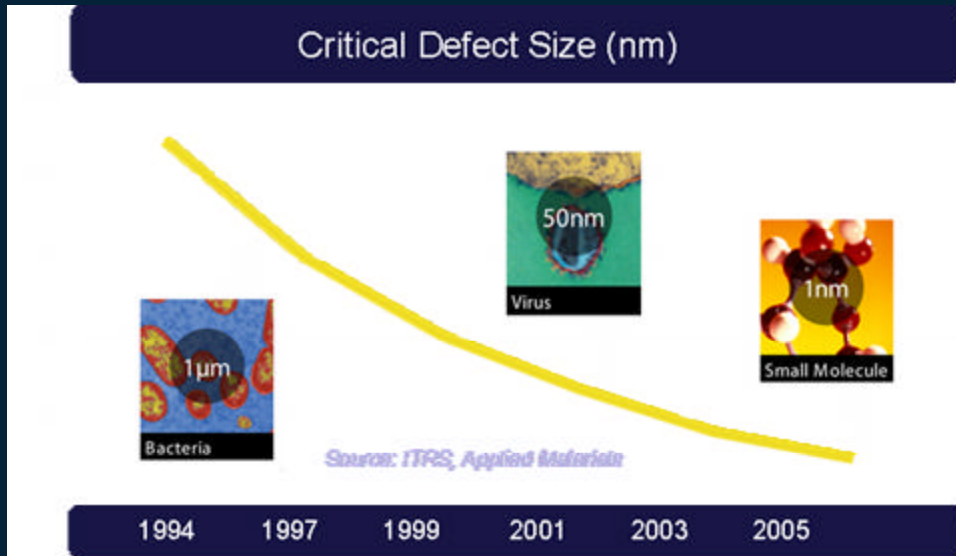
1 H 1.0079																	2 He 4.0026
3 Li 6.941	4 Be 9.0122																
11 Na 22.990	12 Mg 24.305	13 Al 26.981	14 Si 28.086	15 P 30.974	16 S 32.06	17 Cl 35.45	18 Ar 39.948										
19 K 39.098	20 Ca 40.078	21 Sc 44.956	22 Ti 47.867	23 V 50.942	24 Cr 51.996	25 Mn 54.938	26 Fe 55.845	27 Co 58.933	28 Ni 58.693	29 Cu 63.546	30 Zn 65.38	31 Ga 69.723	32 Ge 72.64	33 As 74.922	34 Se 78.96	35 Br 79.904	36 Kr 83.798
37 Rb 85.468	38 Sr 87.62	39 Y 88.906	40 Zr 91.224	41 Nb 92.906	42 Mo 95.94	43 Tc (98)	44 Ru 101.07	45 Rh 101.07	46 Pd 106.4	47 Ag 107.87	48 Cd 112.41	49 In 114.82	50 Sn 118.71	51 Sb 121.76	52 Te 127.6	53 I 126.91	54 Xe 131.29
55 Cs 132.91	56 Ba 137.33	57-71 * 178.49	72 Hf 178.49	73 Ta 180.95	74 W 183.84	75 Re 186.21	76 Os 190.23	77 Ir 192.22	78 Pt 195.08	79 Au 196.97	80 Hg 200.59	81 Tl 204.38	82 Pb 207.2	83 Bi 208.98	84 Po 209	85 At 210	86 Rn 222
87 Fr (223)	88 Ra (226)	89-103 Ac															
57 La 138.91	58 Ce 140.12	59 Pr 140.91	60 Nd 144.24	61 Pm (145)	62 Sm 150.36	63 Eu 151.96	64 Gd 157.25	65 Tb 158.93	66 Dy 162.50	67 Ho 164.93	68 Er 167.26	69 Tm 168.93	70 Yb 173.05	71 Lu 174.967			
89 Ac (112)	90 Th 232.04	91 Pa 231.04	92 U 238.03	93 Np (237)	94 Pu (244)	95 Am (243)	96 Cm (247)	97 Bk (247)	98 Cf (251)	99 Es (252)	100 Fm (257)	101 Md (258)	102 No (259)	103 Lr (262)			

**Source: Intel – ISTAC Meeting 2-2004**

# Integrated Hi-k/Metal Gate CMOS



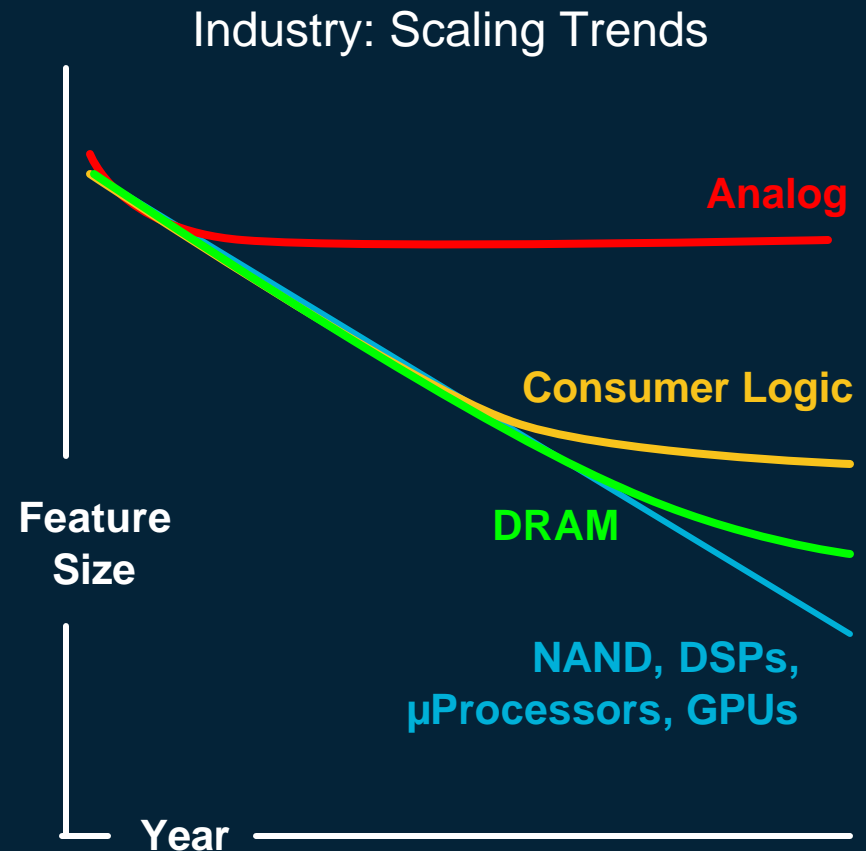
# Require Nanoscale Resolution and Throughput



# Two Key Semiconductor Market Trends

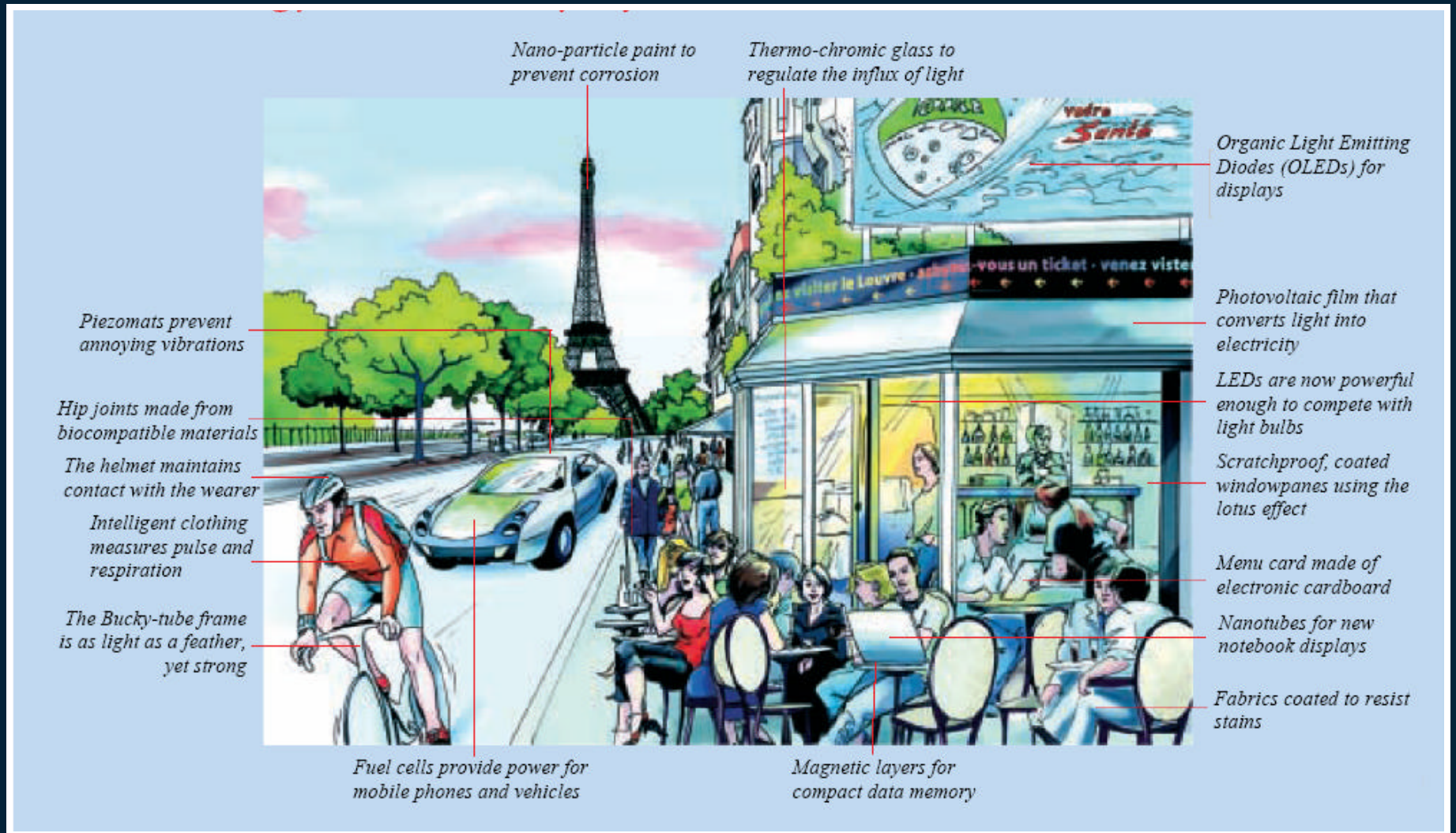
Semiconductor content in electronics, units and transistors all continue to increase but:

- Accelerated consolidation of wafer manufacturers
  - Foundries vs. IDMs
  - Memory oversupply
  - Process R&D costs
- Fewer product families aggressively follow Moore's law
  - Application drivers
  - Developing economies
  - Performance compromises
  - Design costs





# Promise of Nanotechnology



European Commission, Nanotechnology Innovation for Tomorrow's World, Research DG, 2004.

# Nanomanufacturing Technology

## Small features on a large production scale



Placing a nanotube?

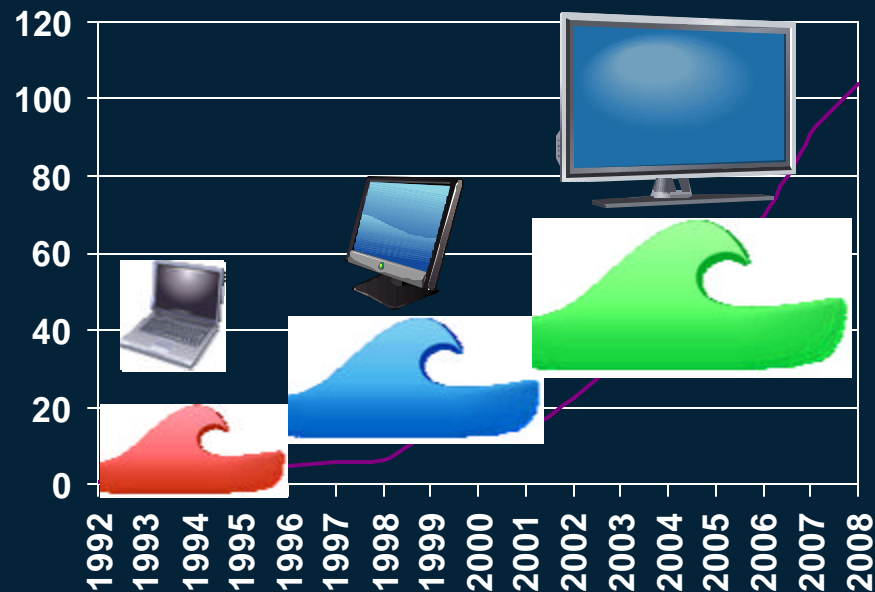


**More Than Nanofabrication – Repeatable, Robust, Reliable,  
Controllable and Cost Effective**

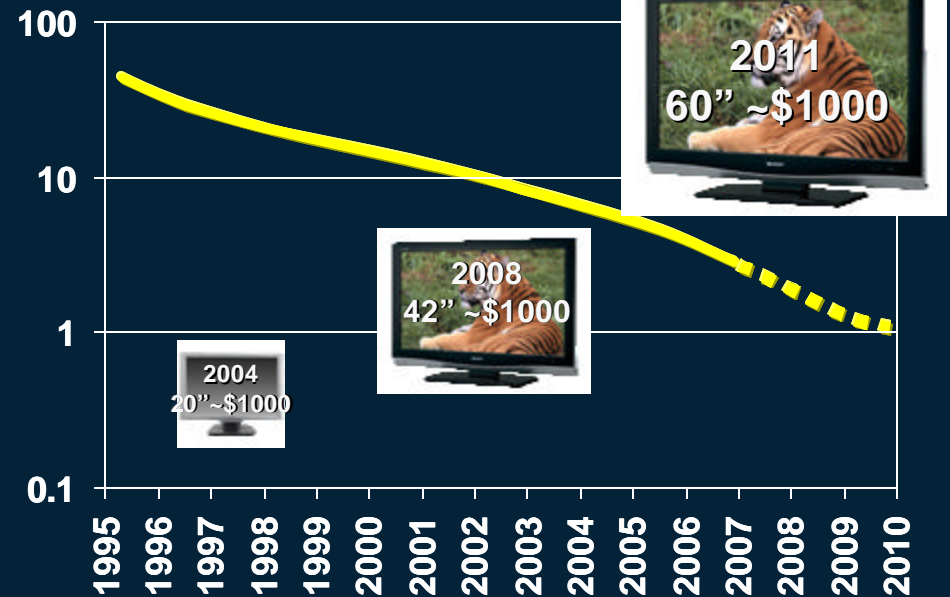


# Flat Panel Display (LCD) Manufacturing

## LCD Industry Revenue (\$B)

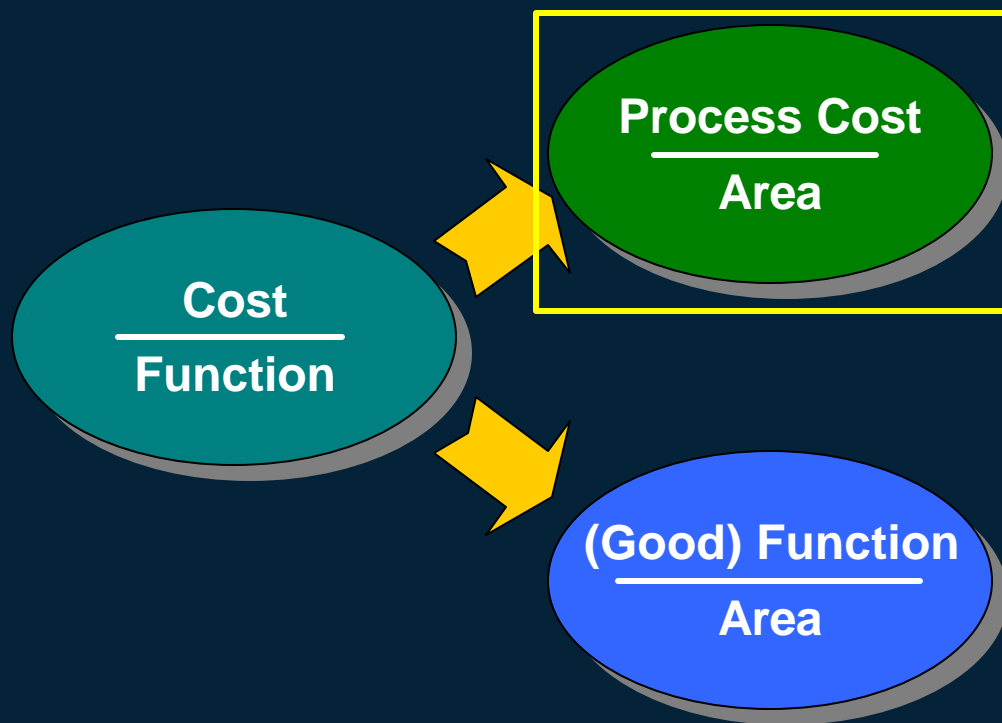


## Production Cost per Area (k\$/m<sup>2</sup>)



> 20% Bigger (HD)TV Every Year for the Same Price






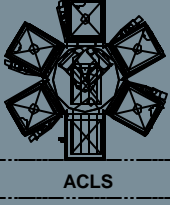

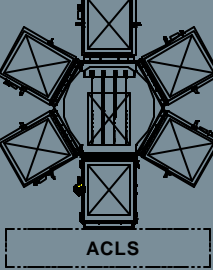
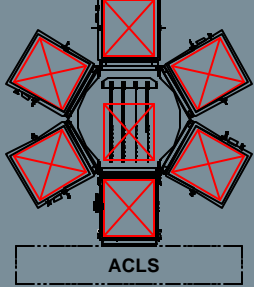
# Cost Per Function: Flat Panel Displays



Cost per area tends to be an equivalent or predominant factor in applications other than VLSI

# Flat Panel Display Equipment – PECVD



	Gen 2	Gen 3 / 3.5	Gen 4	Gen 5	Gen 5	Gen 5.5	Gen 6	Gen 7 / 7.5	Gen 8
1st Release	2/ '93~	4/ '95~	1/ '00~	8/ '01~	6/ '02~	8/ '04~	5/ '03~	7/ '04~	2006
System Layout									

**Gen 10 = 60nm uniformity over  $\sim 10^{19}$  nm<sup>2</sup> area at 50sph**

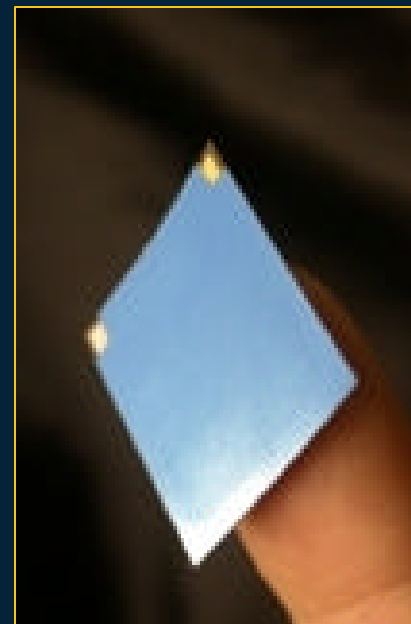
# Nanotechnology Opportunities In Energy



**Energy  
Conservation**



**Energy  
Conversion**



**Energy  
Storage**

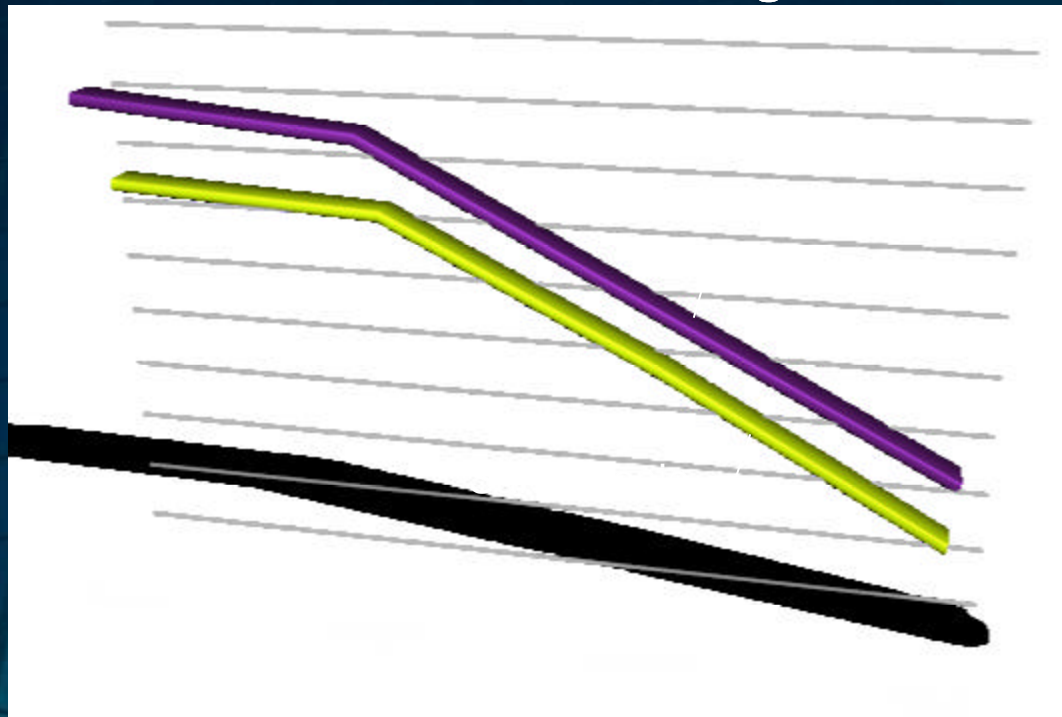
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**Technology to improve performance, form and cost**



# Architectural Coated Glass

## Cost Reductions Achieved with Low-e Coatings



Annual Energy Expenditures (\$)



2000 ft² house with 300 ft² of windows

# Increasing Adoption of Coated Glass

## Bird's Nest Stadium (Beijing)

Shanghai SYP Engineering Glass Co.  
10,000m<sup>2</sup> of high performance Low-E glass



## Burj Dubai (UAE)

Guardian Industries  
100,000m<sup>2</sup> SunGuard® Solar Control  
and Low-E coated glass



## Main Triangle Building (Frankfurt)

Guardian Industries  
15,000m<sup>2</sup> SunGuard® Solar Control  
and Low-E coated glass



## House of Sweden (Washington DC)

AGC Flat Glass  
5500m<sup>2</sup> Stopray® Elite  
and Stopray® Carat glass



## Savings from 2007 Global Output ~ 36,000 Bbl/day†

† Equivalent to 12 oil wells or 18Mt CO<sub>2</sub>



# Large Area Glass Coating Systems



- Glass Substrate is ~ 2.6 m x 3.6 m
  - Uniformity Spec of +/- 1% on 275 nm film (10 layer Triple Low e stack)
- 18 Chamber System ~ 90m: one panel every 20 sec
  - Output per month ~ 7Mft<sup>2</sup>

# Electrochromic "Smart Glass"



## Key Requirements for Market Adoption:

- **Performance:** Energy efficiency, lifetime
- **Form:** Color selection, match non-EC panes, pane-to-pane consistency, large size panes, on-off
- **Cost:** At least comparable to Low-e glass + shades

## Typical Structure

- ~ 10 metal/dielectric layers, most < 100nm thick (up to ~ 500nm)

Images courtesy of Sage Electrochromics

# Primary Commercial Solar PV Markets



## Residential

**Today's Installed Base**  
5.4 GW

### Market Drivers

- High utility bills
- Availability of incentives
- Green choice



## Commercial Rooftop

**Today's Installed Base**  
4.2 GW

### Market Drivers

- High utility bills
- Unpredictable cost
- Under-utilized urban space



## Utility Scale

**Today's Installed Base**  
5.4 GW

### Market Drivers

- Solar economics
- Favorable tax policy
- Unpredictable fuel and carbon costs

**Total new PV installations in 2008 ~4.1 GW**

Source: Navigant 2007, 2008, Marketbuzz 2008



# Mainstream PV Technologies

## Crystalline Silicon

Preferred for residential applications



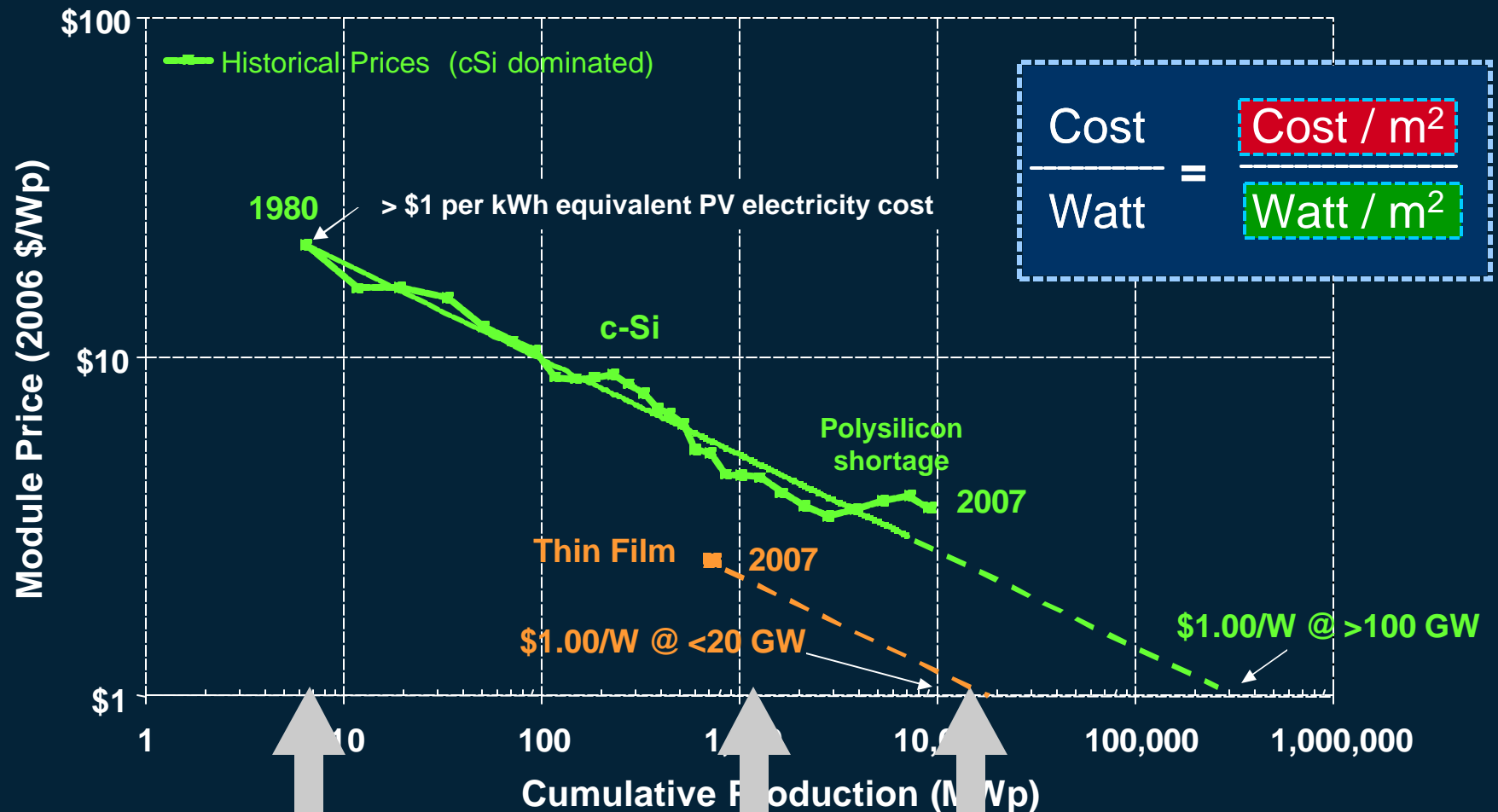
## Thin Film

Preferred for large scale applications



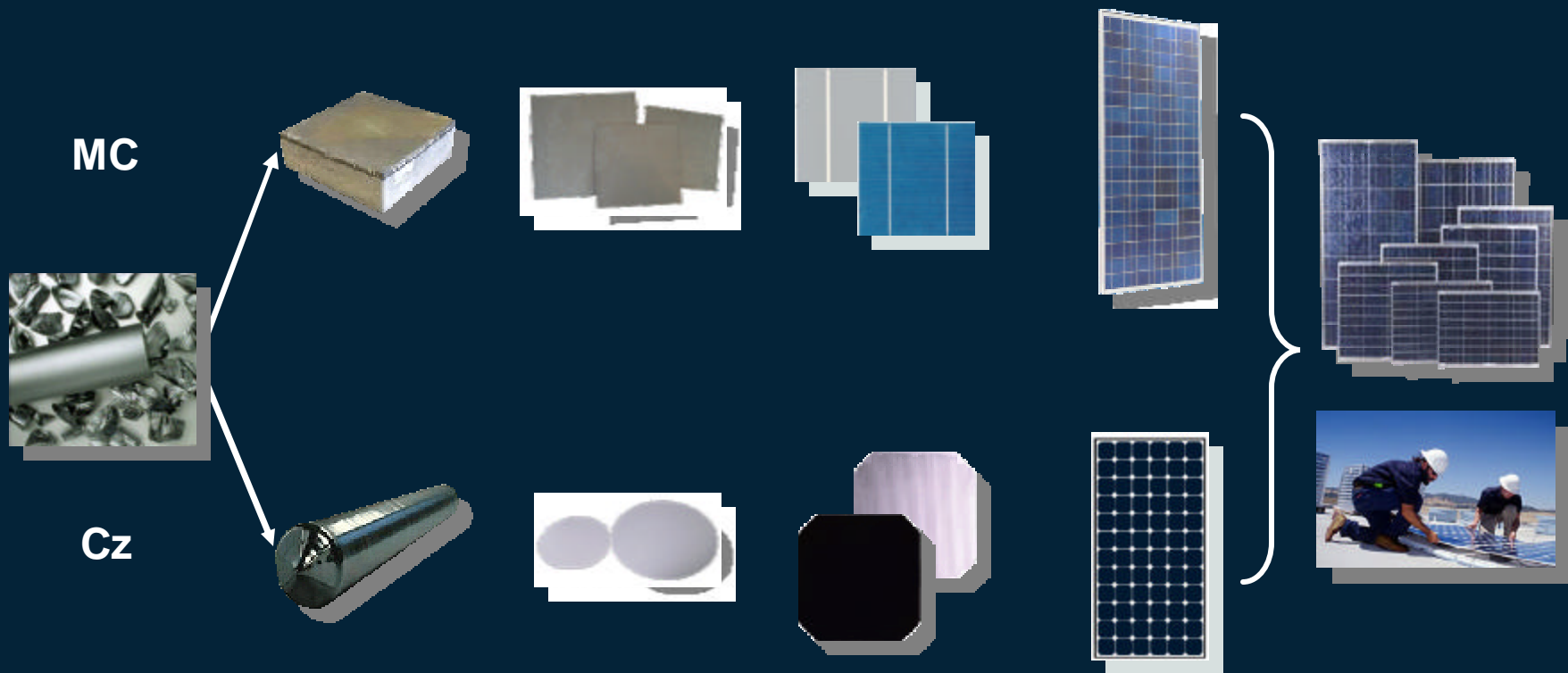
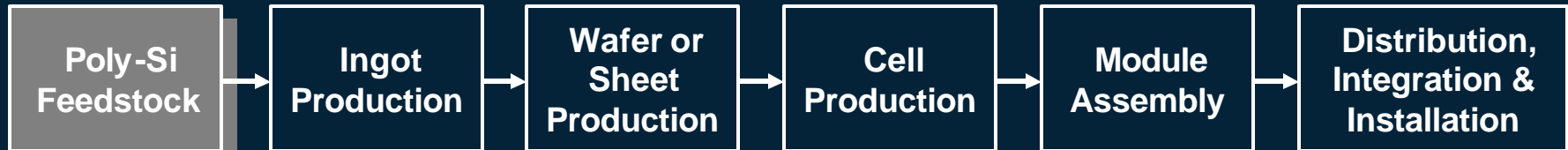
**Common focus to drive down cost per watt**

# Solar Learning Curve: Module Cost/Watt



Production line size (Megawatts per Year)	0.5 (1980)	5 (2000)	50 (2005)	100 (2010)
Lines Per Factory	2	3	4	10

# Crystalline Silicon PV Value Chain

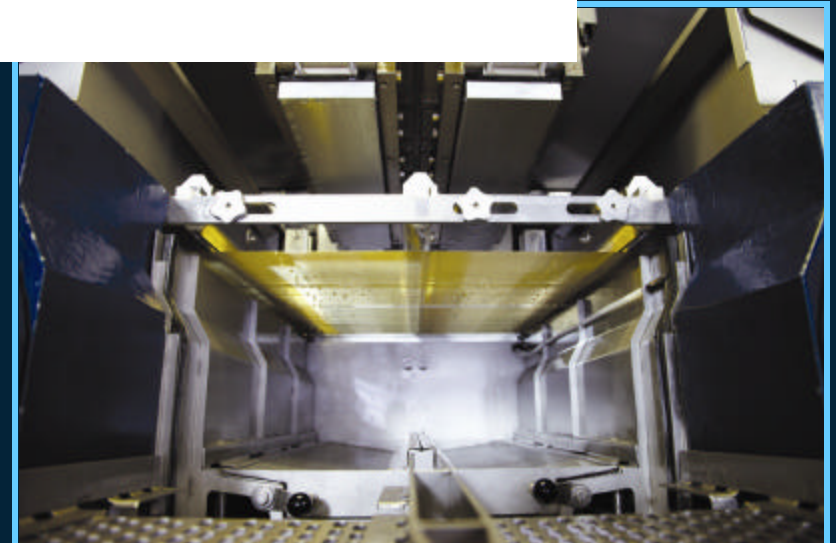




# Improve Material Efficiency: Thin Wafers

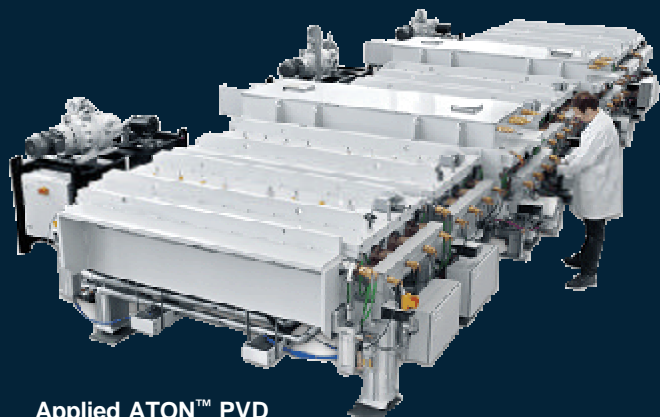
Cost / m<sup>2</sup>

Watt / m<sup>2</sup>



\* Cost assumes fixed silicon costs at \$55/kg and constant efficiency

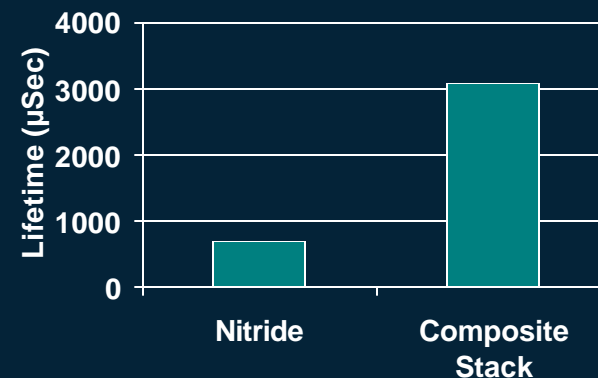
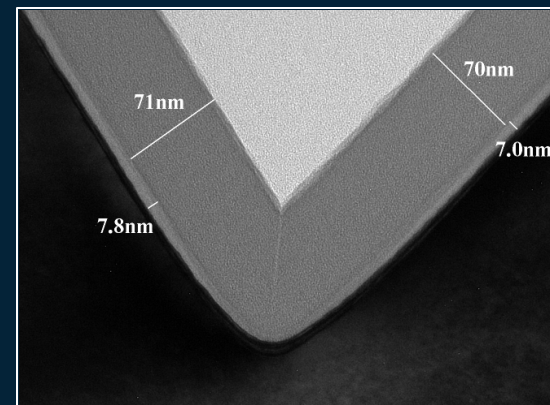
# High Productivity ARC/Passivation



Cost / m<sup>2</sup>

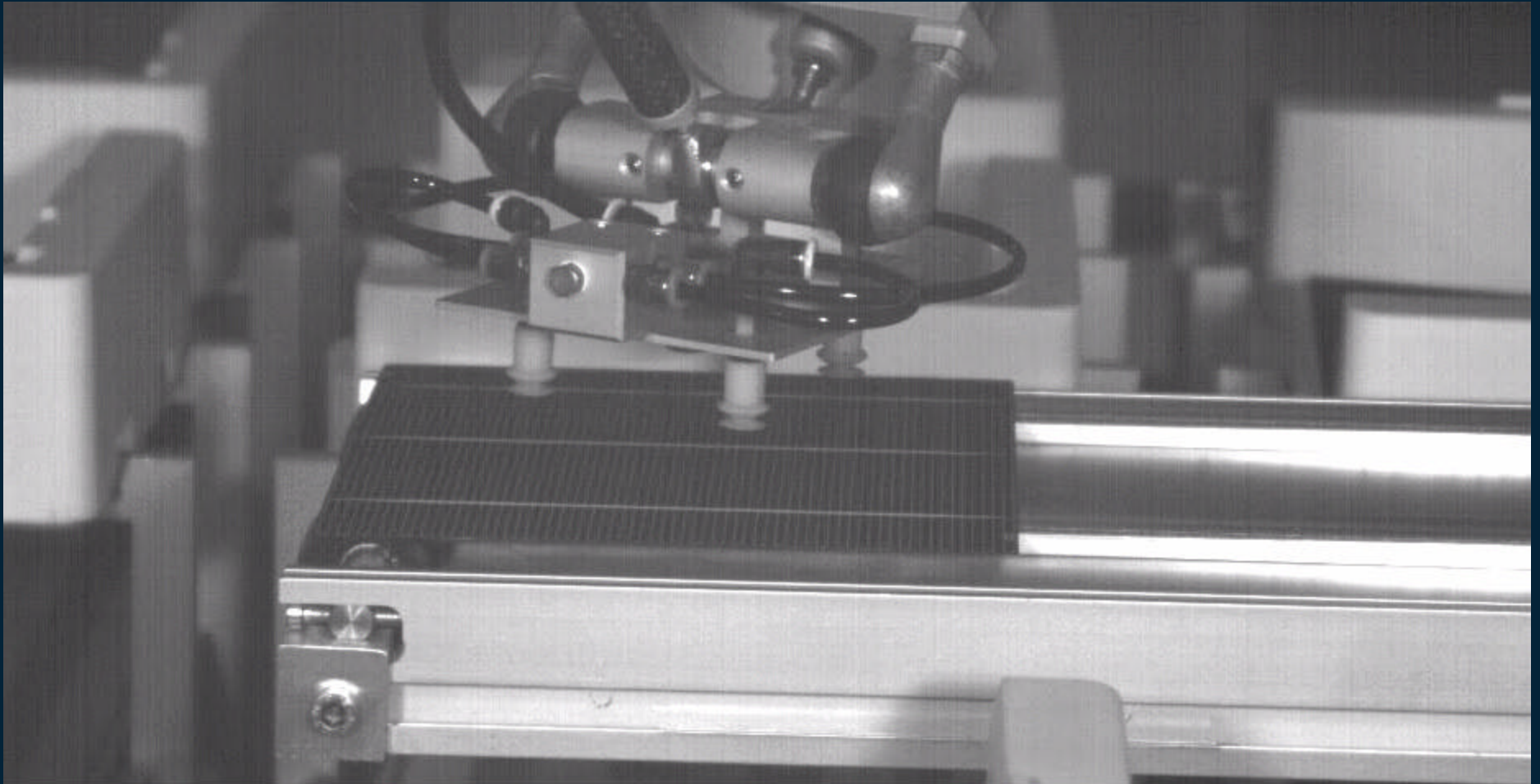
Watt / m<sup>2</sup>

- Yield
- Thruput
- Uptime
- Thin wafers
- COC
- Efficiency
- Uniformity



- Low Interface State Density
- Optically Transparent
- Stable After Contact Firing

# Thin Wafer Processing



0100 -1647,2[ms] [1075 Hz] SpeedCam MiniVis

# Thin Film PV Value Chain

