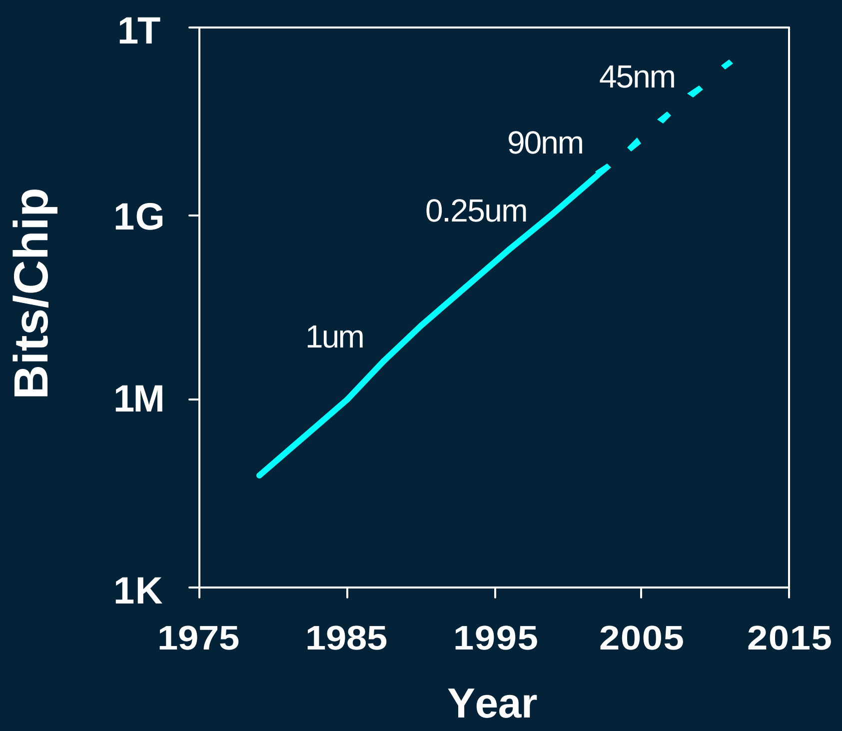
MARK PINTO, PH.D.

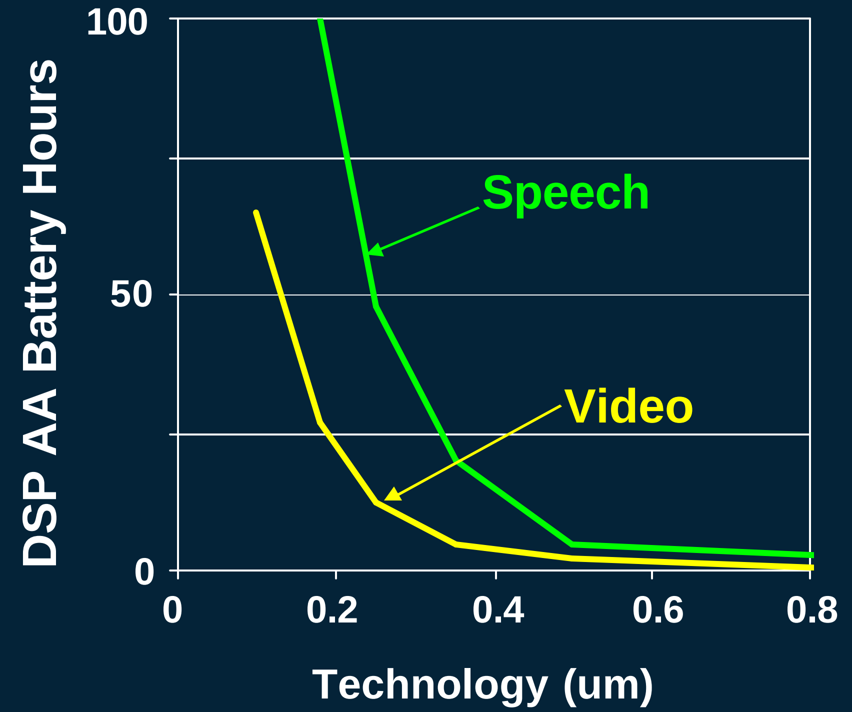
NANOMANUFACTURING TECHNOLOGY

NAS/SSSC Spring Meeting
April 2, 2009

APPLIED MATERIALS.

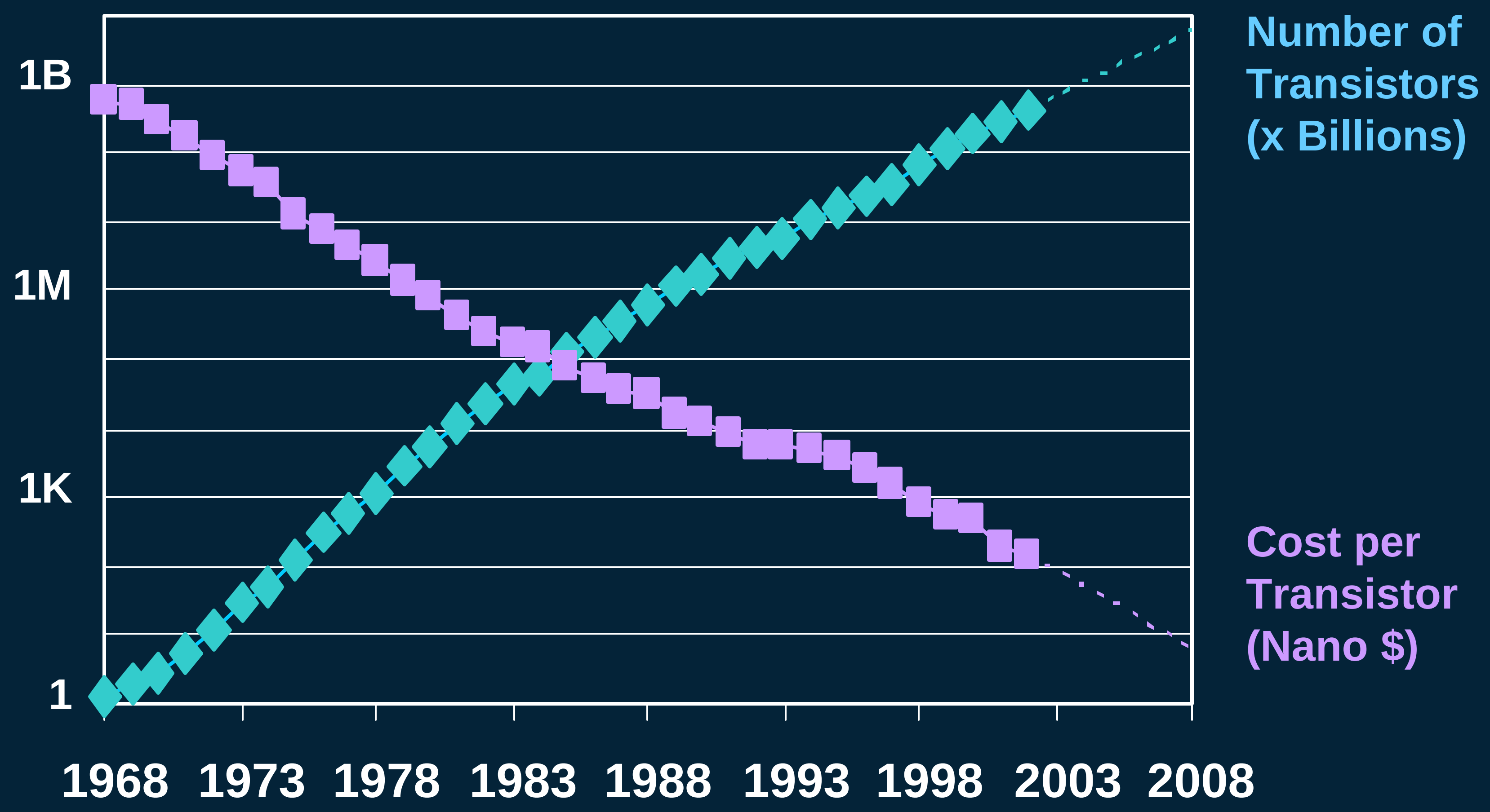
Moore's Law and Transistor Scaling





- Decrease transistor dimensions by k, drop voltage by k
- Circuit area reduced by 1/k2, speed increased by k
- Power per circuit reduced by 1/k2, power per area constant

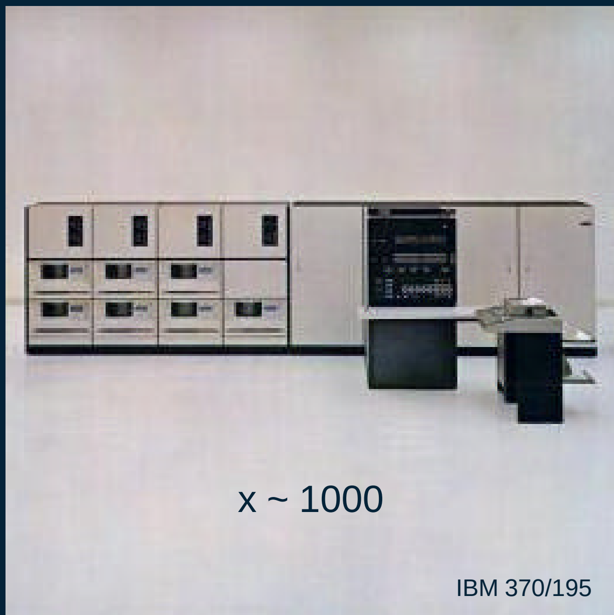
Moore's Law and Transistor Cost

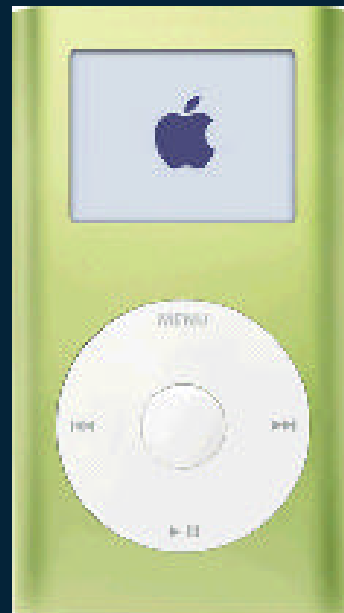


(Source: G. Moore, ISSCC 2003)

APPLIED MATERIALS

A Recent Product Enabled by Nanoelectronics



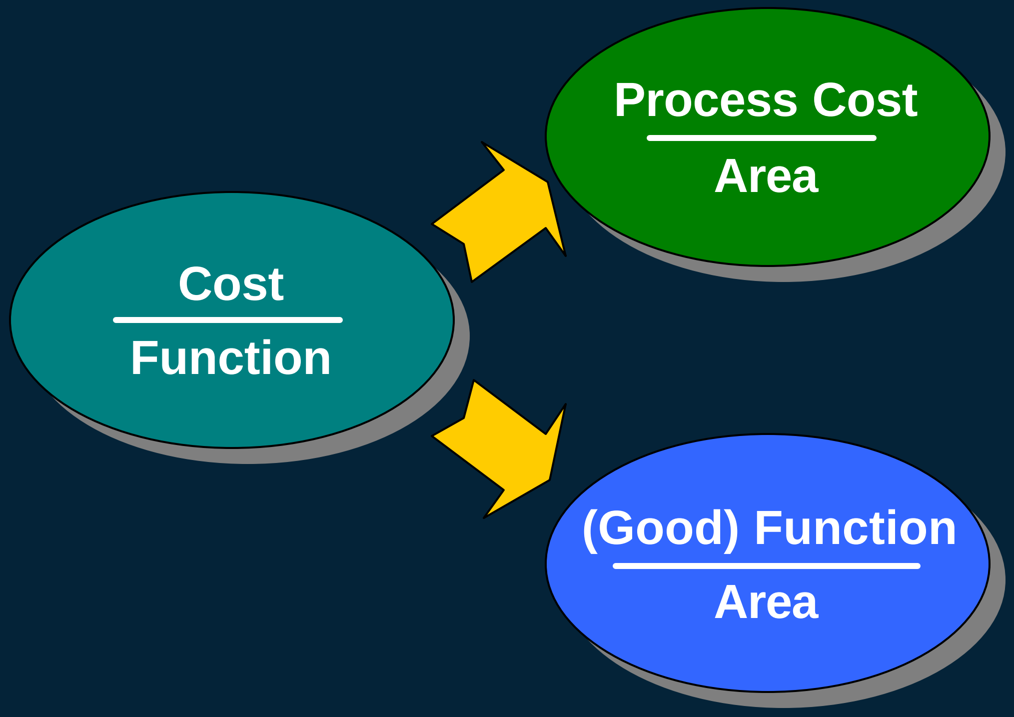


1975 = $1B† **2006 ~ $200** **2020 = 5¢***

† Memory cost only

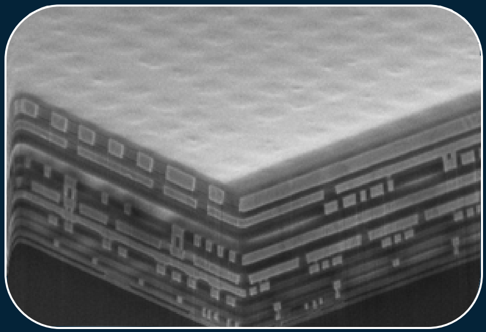
* Extrapolating memory cost reduction factor over last 30 years and display cost/area over last 10 years

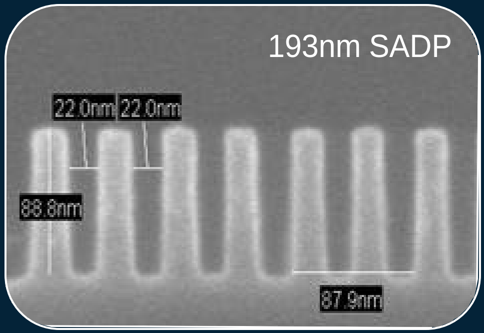
Cost Per Function



APPLIED MATERIALS

Cost Per Function: VLSI Technology





ost
nction

Process Cost
Area

(Good) Function
Area

Scaling has been the primary cost driver for ICs – but not at an overcompensating increase in process cost/area

APPLIED MATERIALS

Patterning Is More Than Printing

PRODUCTIVITY

- Automation
- eDiagnostics
- Material Handling
- Reticle Management

PREPARATION

Patterning Films

- CVD Hardmask
- CVD ARC/Spin-on ARC
- PVD Hardmask

Planarity Enhancement

- Ecmp
- Real-Time Profile Ctrl
- Fixed-Abrasive CMP

PRINTING

- Scanner
- Track
- Mask/Mask Etch
- Photoresist
- K_1 reduction

PATTERN TRANSFER

Etch

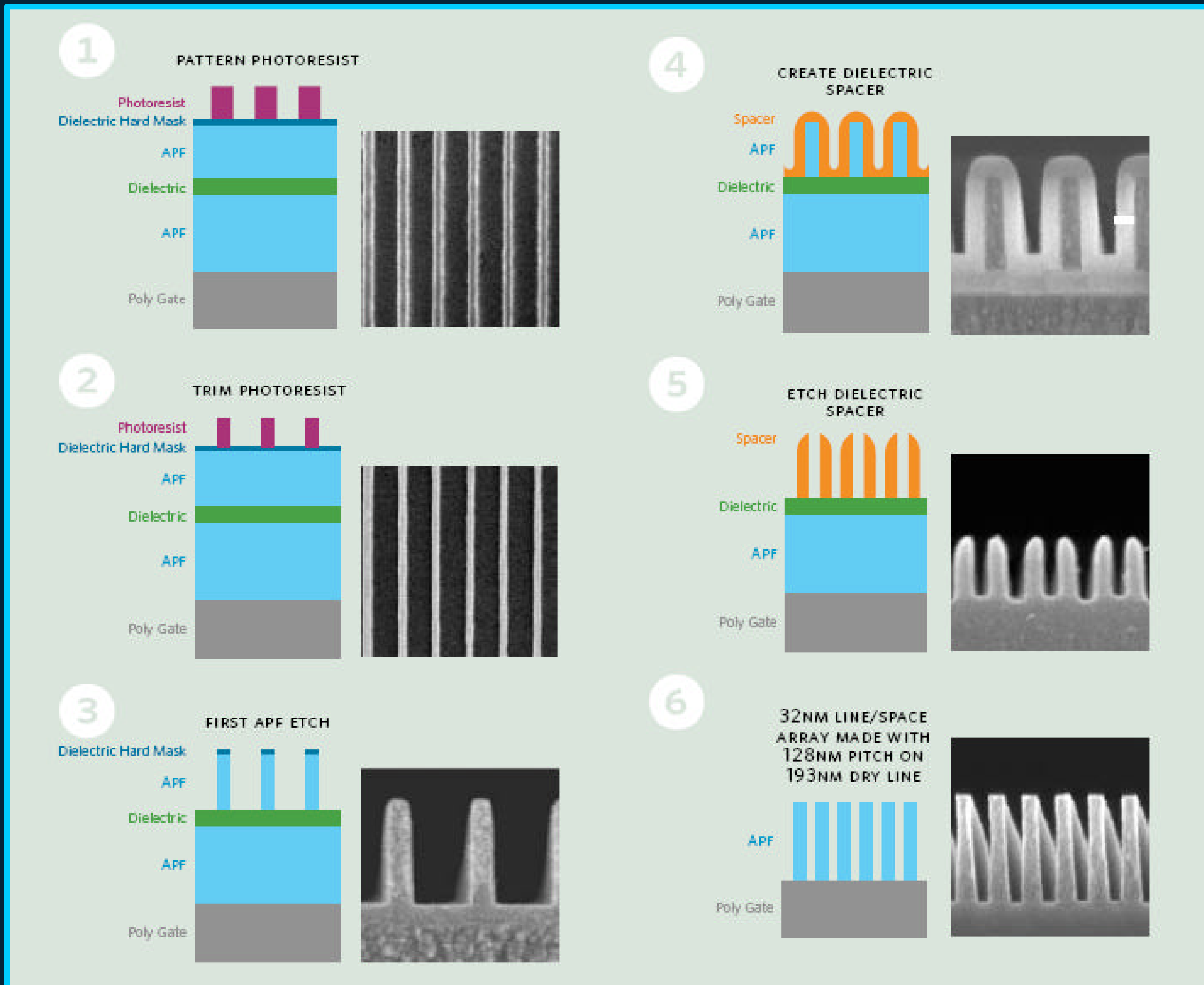
- High Aspect Ratio Etch
- Critical Etch
- Damascene Etch
- Trimming

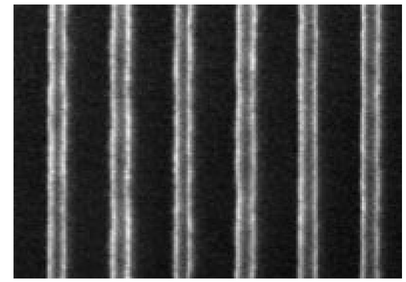
PROCESS CONTROL/DFM

- CD SEM
- OPC Qualification
- APC
- Defect Inspection and Review
- Overlay

APPLIED MATERIALS

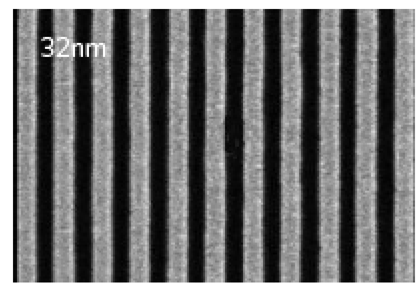
Self Aligned Double Patterning





after lithography

LER = 3.1nm (3s)



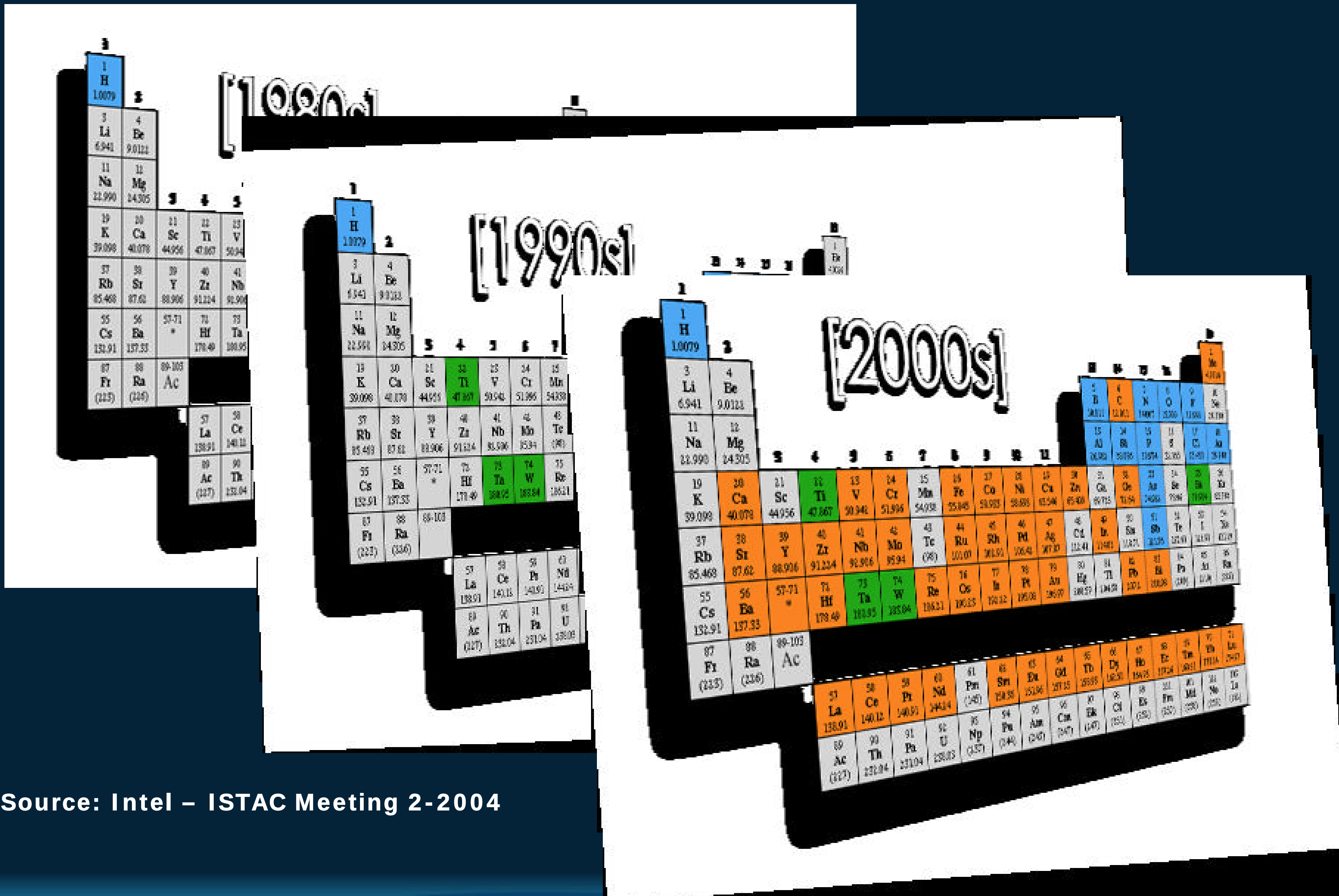
after final APF etch

LER = 1.5nm (3s)

EXTERNAL USE

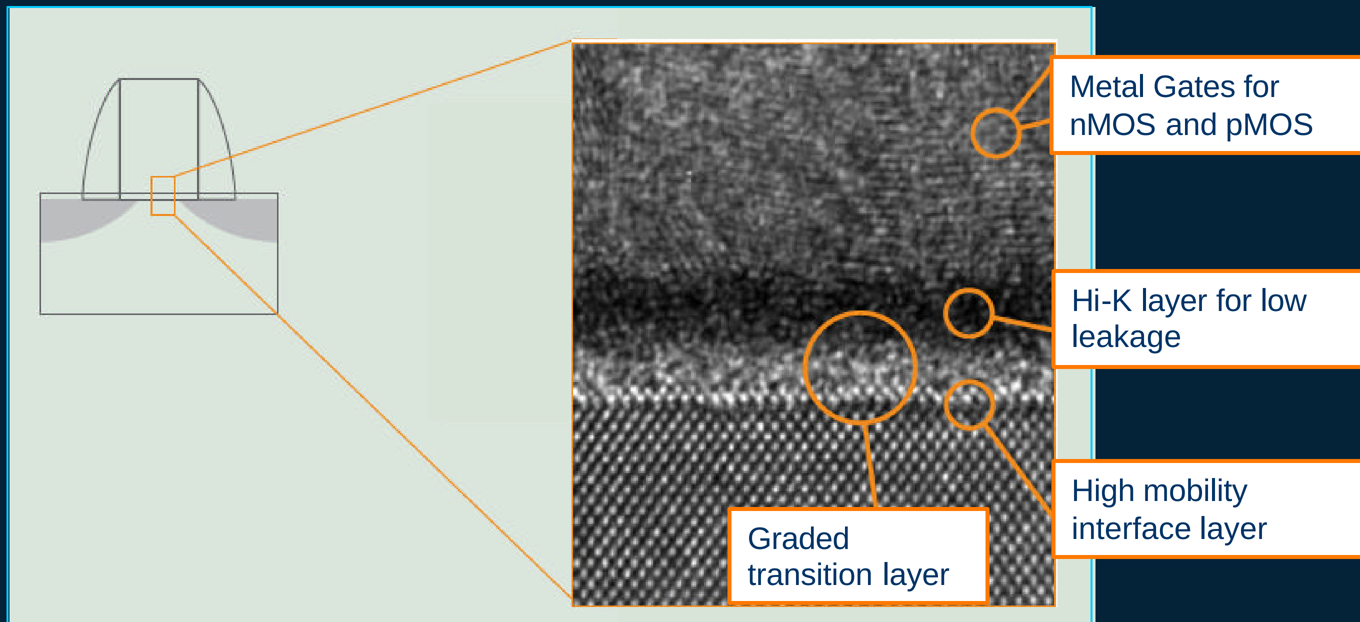
APPLIED MATERIALS

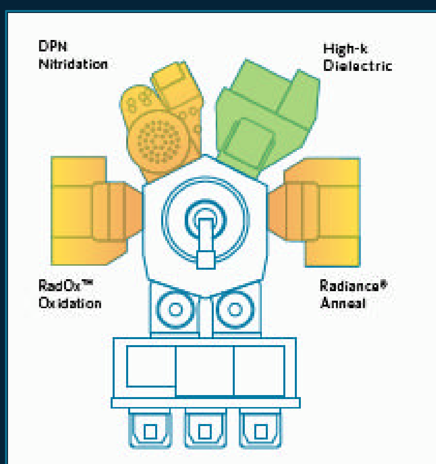
Progress Through Materials Innovation

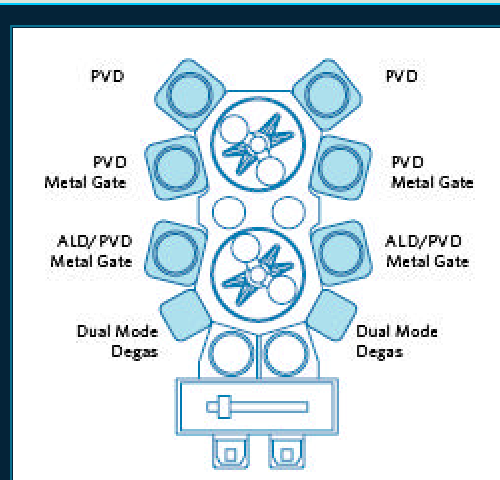


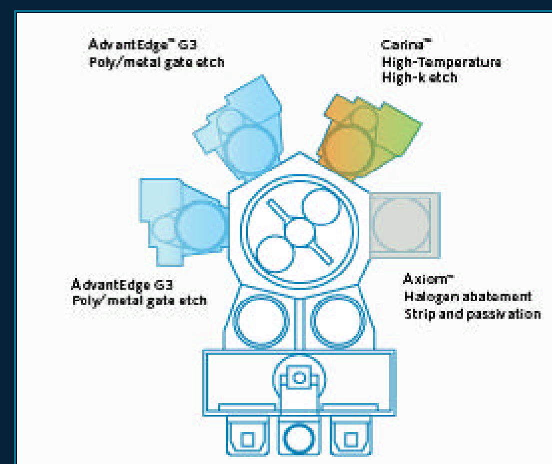
Source: Intel – ISTAC Meeting 2-2004

Integrated Hi-k/Metal Gate CMOS



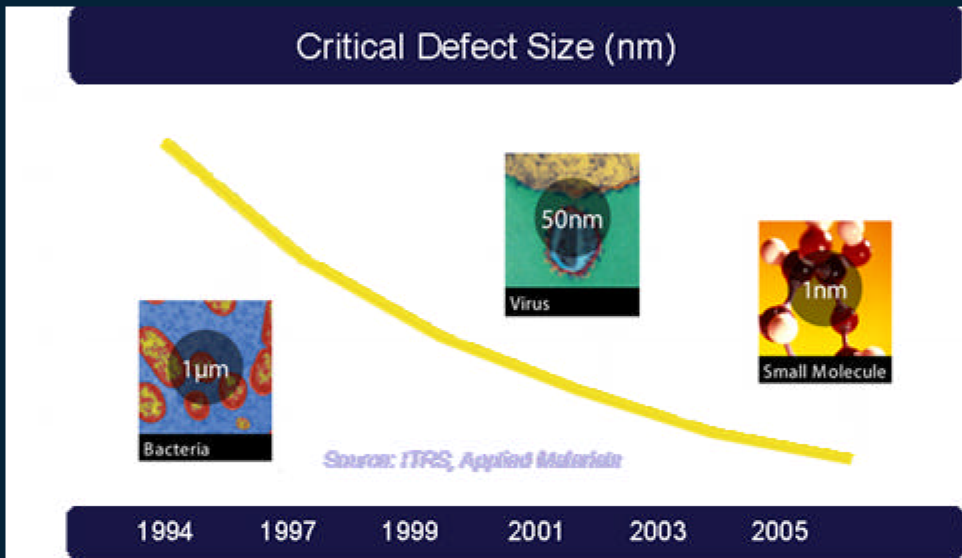


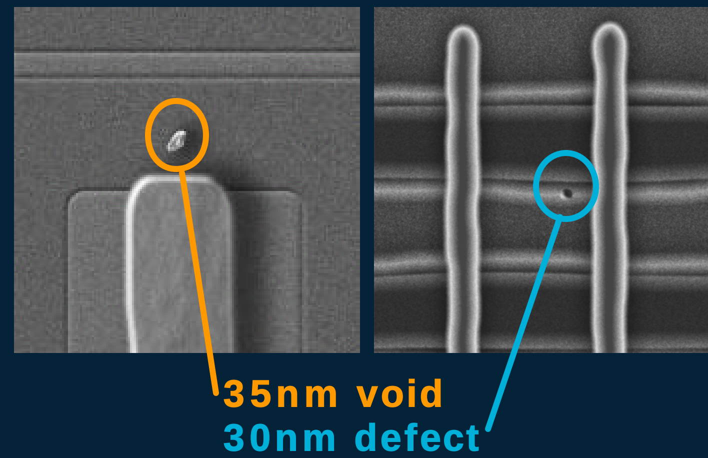


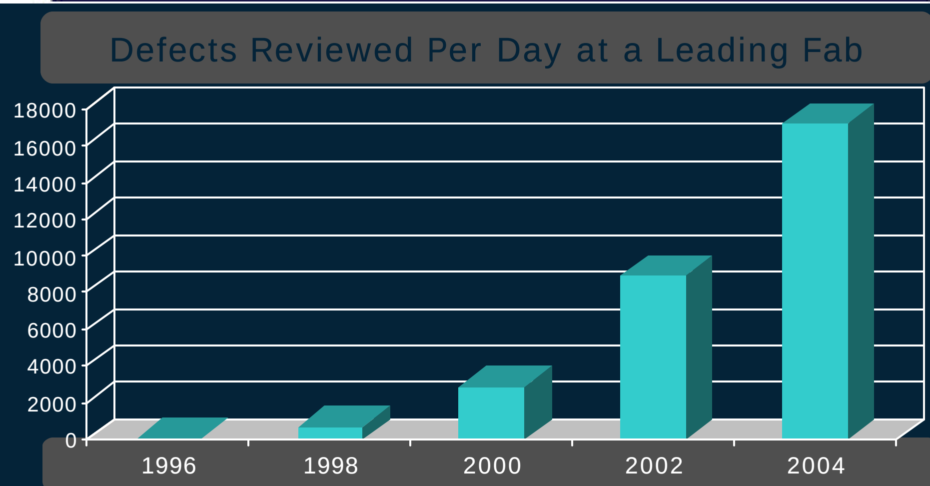


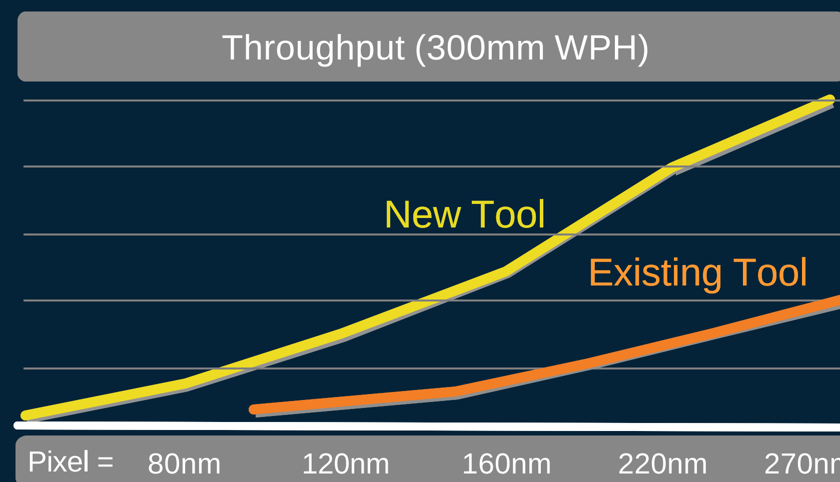
APPLIED MATERIALS

Require Nanoscale Resolution *and* Throughput









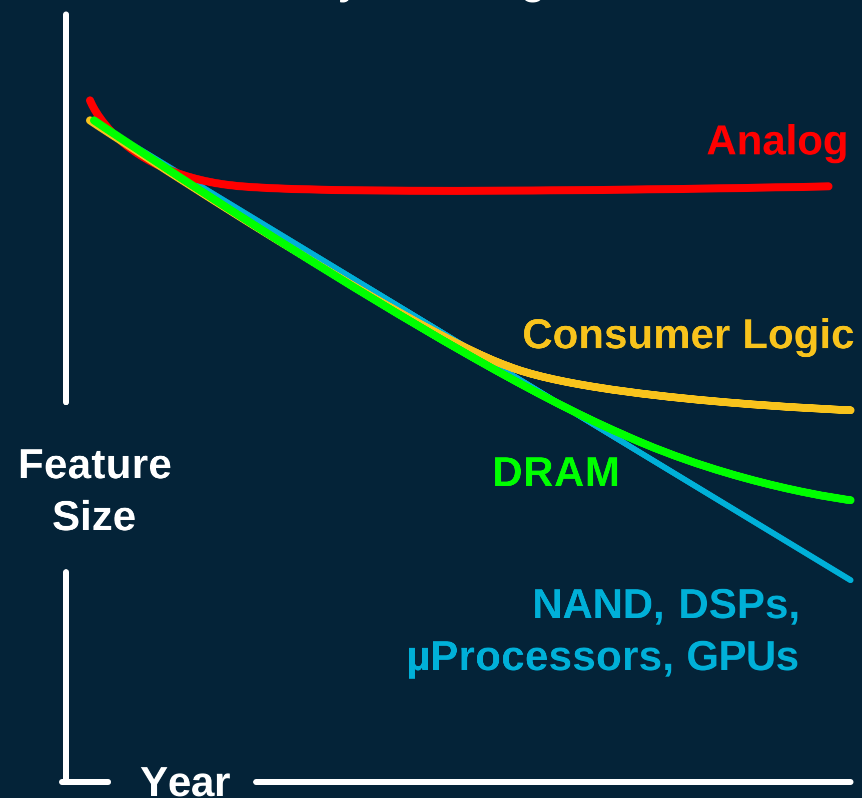
EXTERNAL USE

Two Key Semiconductor Market Trends

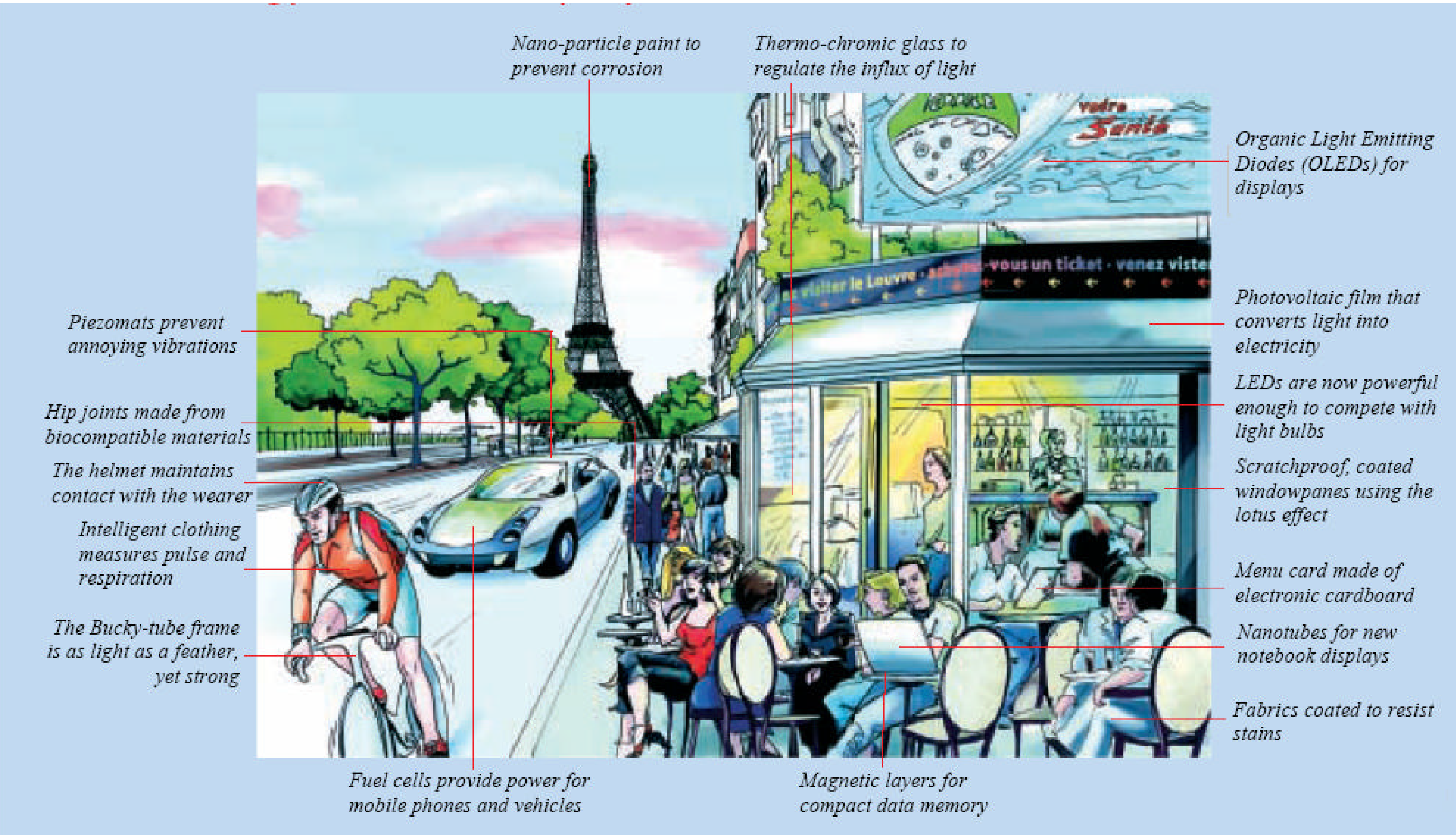
Semiconductor content in electronics, units and transistors all continue to increase but:

- Accelerated consolidation of wafer manufacturers
  - Foundries vs. IDMs
  - Memory oversupply
  - Process R&D costs
- Fewer product families aggressively follow Moore's law
  - Application drivers
  - Developing economies
  - Performance compromises
  - Design costs

Industry: Scaling Trends



Promise of Nanotechnology



European Commission, Nanotechnology Innovation for Tomorrow's World, Research DG, 2004.

Nanomanufacturing Technology
Small features on a large production scale

Placing a nanotube?

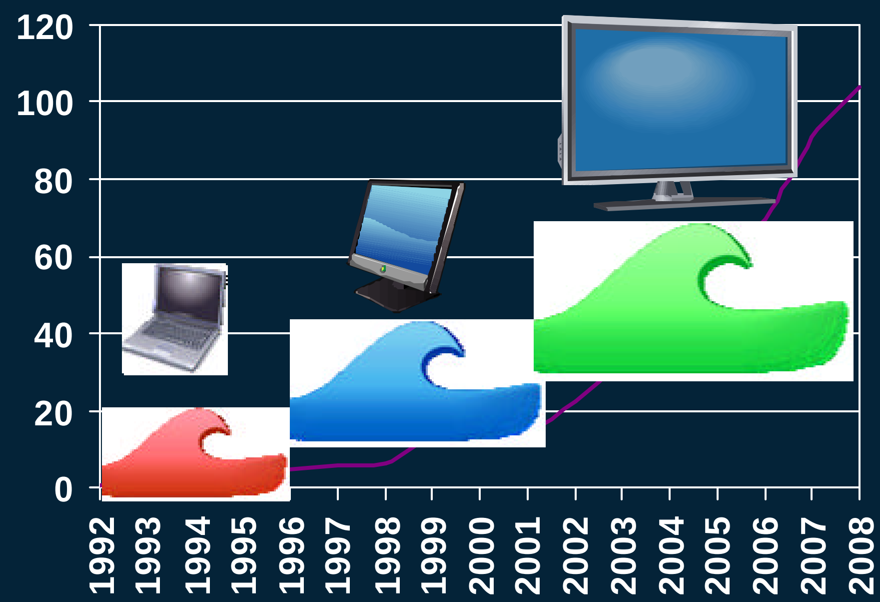
Scale Up?

Additional Innovation

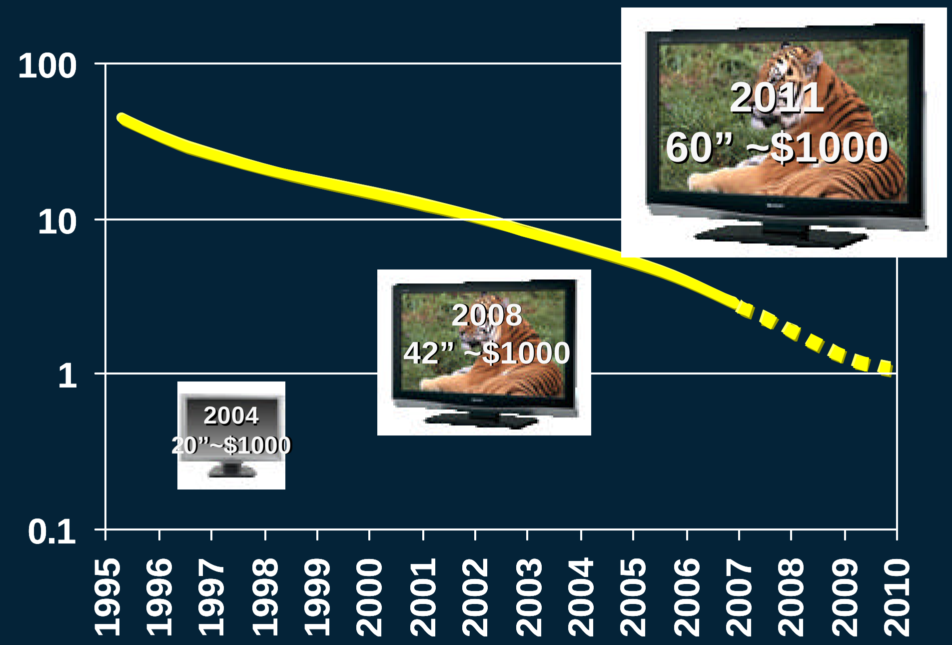
More Than Nanofabrication – Repeatable, Robust, Reliable, Controllable and Cost Effective

Flat Panel Display (LCD) Manufacturing

LCD Industry Revenue ($B)



Production Cost per Area (k$/m²)



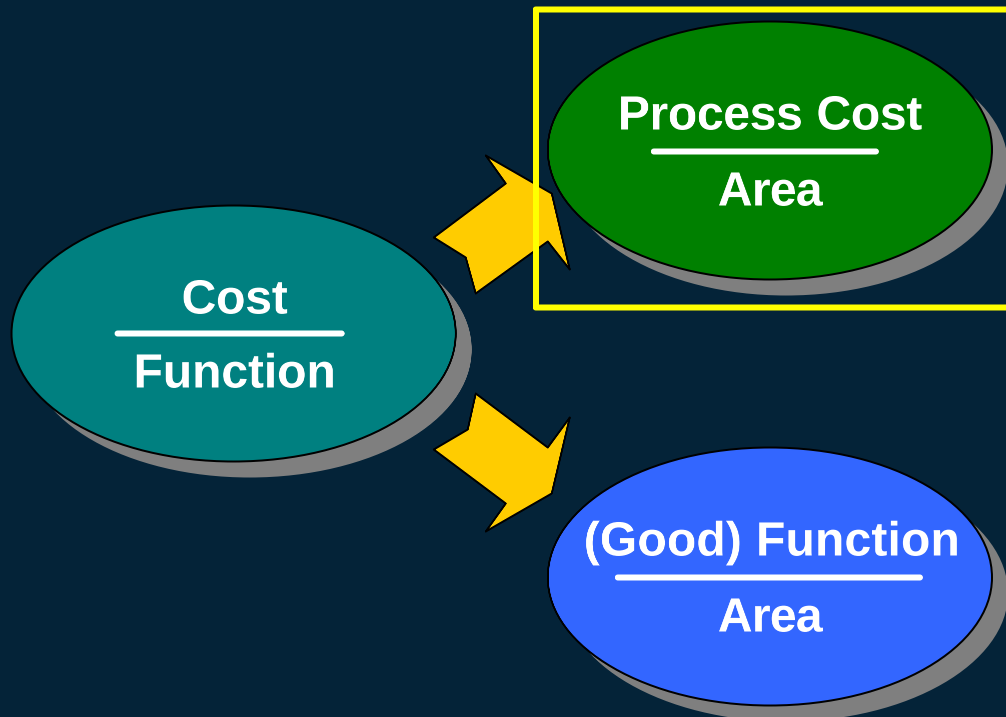
> 20% Bigger (HD)TV Every Year for the Same Price

Cost Per Function: Flat Panel Displays


Applied PECVD 5.7


AKT-PIVOT™ 55KV PVD


Courtesy Sharp

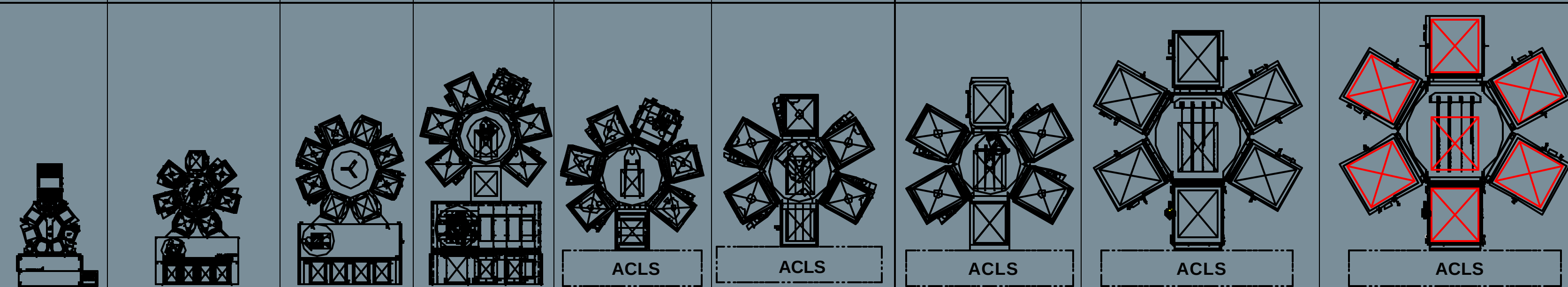


Cost per area tends to be an equivalent or predominant factor in applications other than VLSI

Flat Panel Display Equipment – PECVD

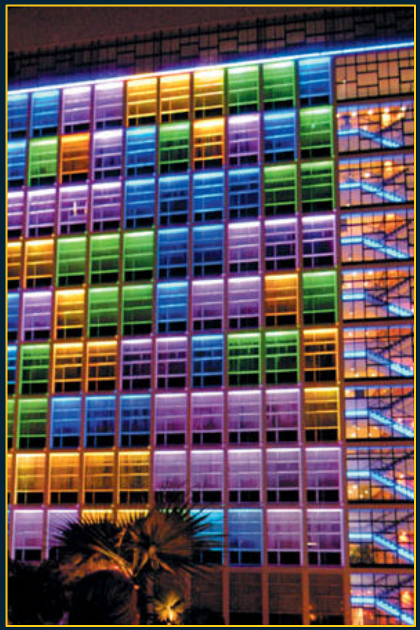
	Gen 2	Gen 3 / 3.5	Gen 4	Gen 5	Gen 5	Gen 5.5	Gen 6	Gen 7 / 7.5	Gen 8
1st Release	2/ '93~	4/ '95~	1/ '00~	8/ '01~	6/ '02~	8/ '04~	5/ '03~	7/ '04~	2006

System Layout



Gen 10 = 60nm uniformity over ~ 10^{19} nm^2 area at 50sph

Nanotechnology Opportunities In Energy



Energy Conservation

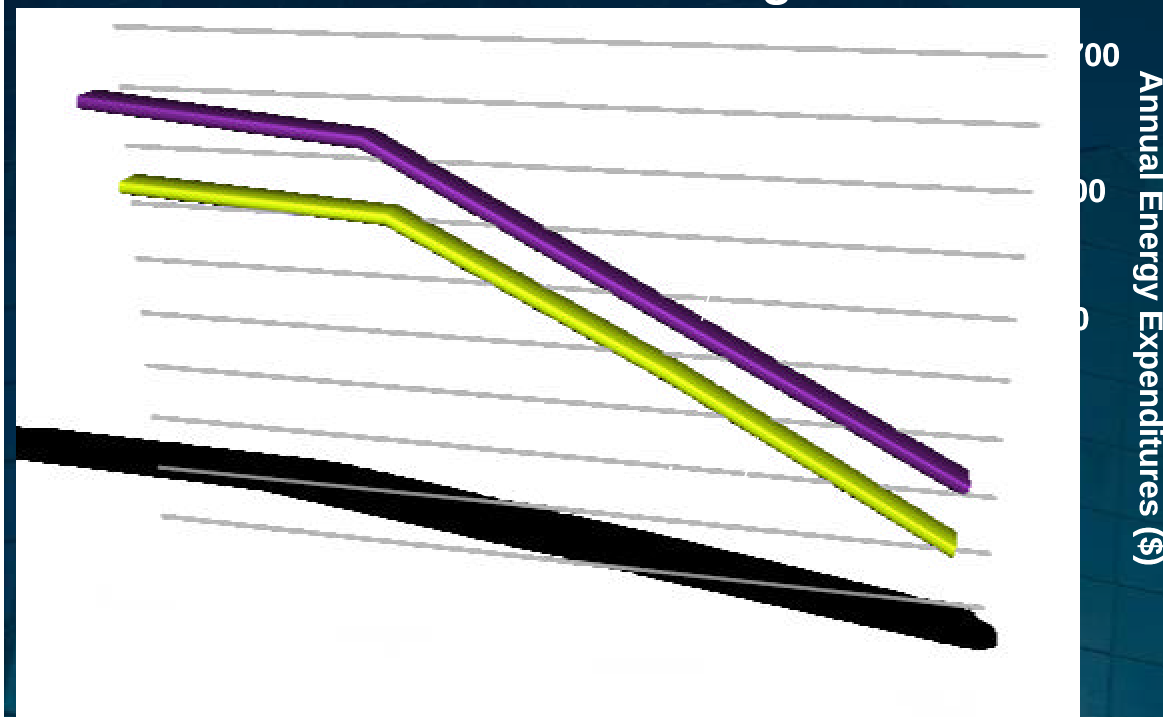
Energy Conversion

Energy Storage

Technology to improve performance, form and cost

Architectual Coated Glass

Cost Reductions Achieved with Low-e Coatings



2000 ft2 house with 300 ft2 of windows

Increasing Adoption of Coated Glass

Savings from 2007 Global Output ~ 36,000 Bbl/day†

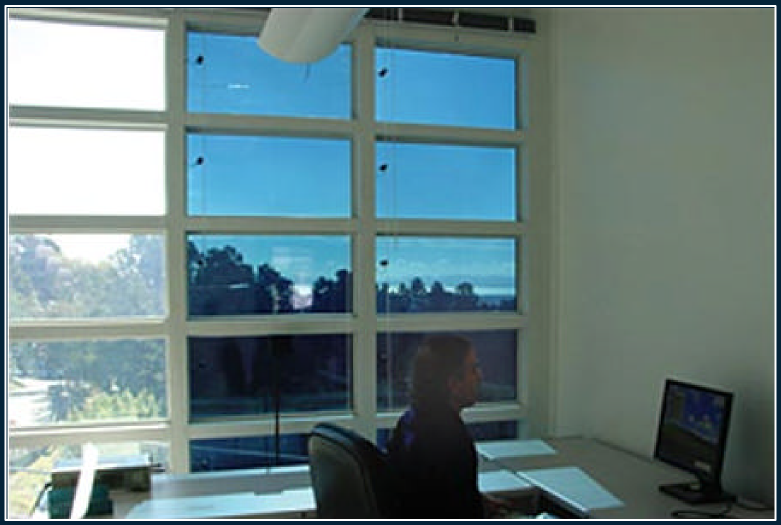
† Equivalent to 12 oil wells or 18Mt CO_2

APPLIED MATERIALS

Large Area Glass Coating Systems

- Glass Substrate is ~ 2.6 m x 3.6 m
  - Uniformity Spec of +/- 1% on 275 nm film (10 layer Triple Low e stack)
- 18 Chamber System ~ 90m: one panel every 20 sec
  - Output per month ~ 7Mft2

Electrochromic "Smart Glass"



Key Requirements for Market Adoption:

- **Performance**: Energy efficiency, lifetime
- **Form**: Color selection, match non-EC panes, pane-to-pane consistency, large size panes, on-off
- **Cost**: At least comparable to Low-e glass + shades

Typical Structure

- ~ 10 metal/dielectric layers, most < 100nm thick (up to ~ 500nm)

Images courtesy of Sage Electrochromics

Primary Commercial Solar PV Markets

Residential

Today's Installed Base
5.4 GW

Market Drivers
- High utility bills
- Availability of incentives
- Green choice

Commercial Rooftop

Today's Installed Base
4.2 GW

Market Drivers
- High utility bills
- Unpredictable cost
- Under-utilized urban space

Utility Scale

Today's Installed Base
5.4 GW

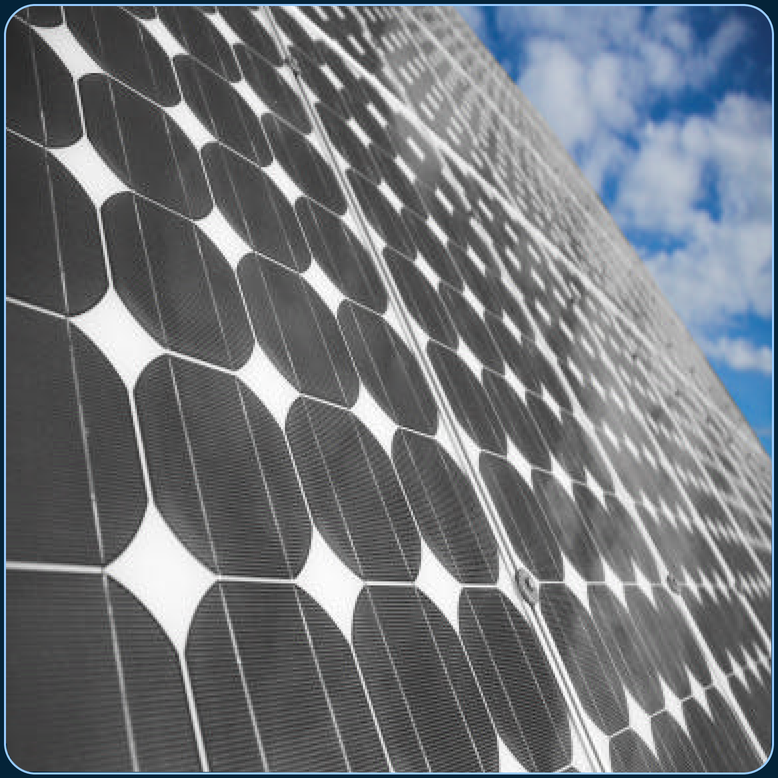
Market Drivers
- Solar economics
- Favorable tax policy
- Unpredictable fuel and carbon costs

Total new PV installations in 2008 ~4.1 GW

Source: Navigant 2007, 2008, Marketbuzz 2008

Mainstream PV Technologies

Crystalline Silicon
Preferred for residential applications

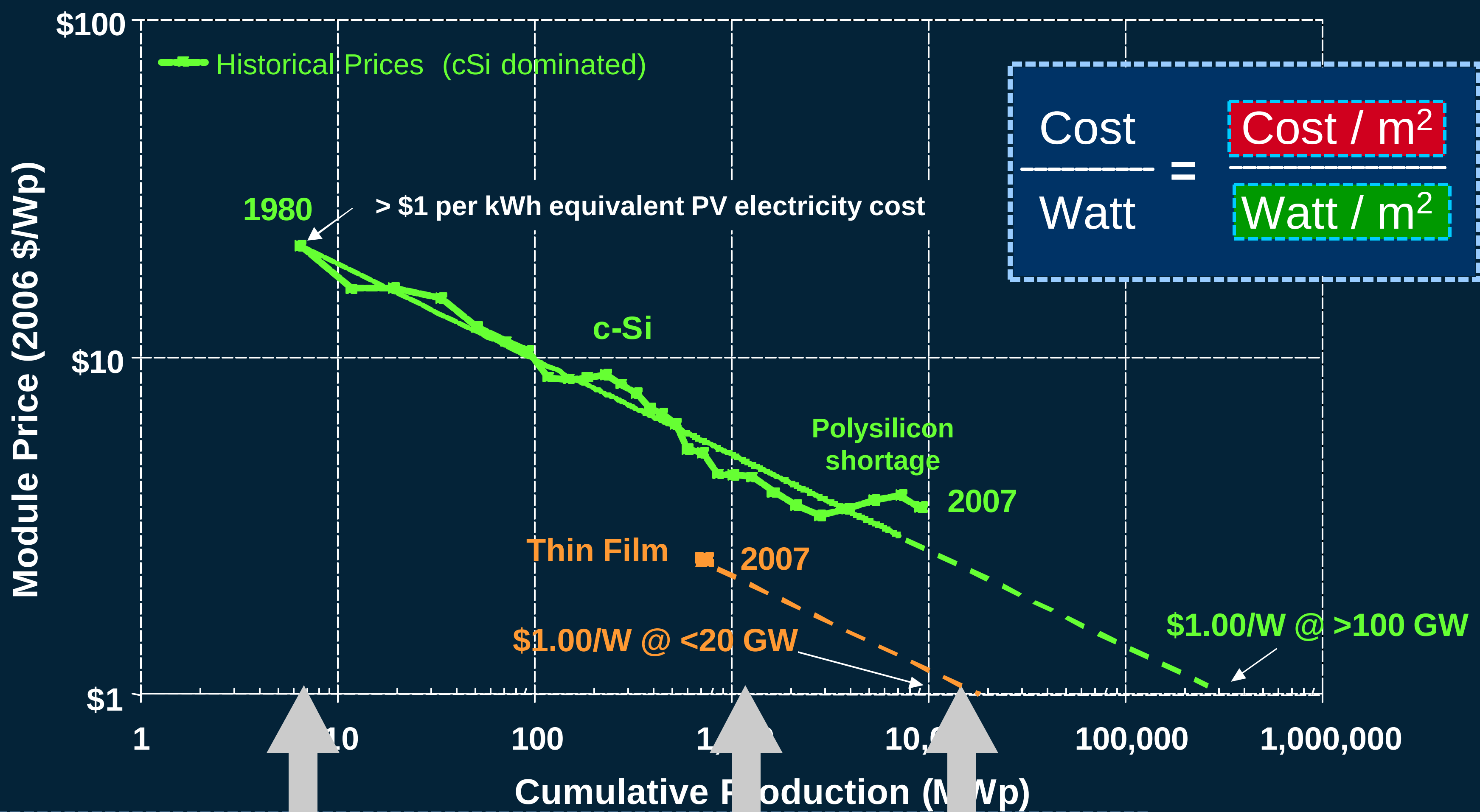


Thin Film
Preferred for large scale applications

Common focus to drive down cost per watt

APPLIED MATERIALS

Solar Learning Curve: Module Cost/Watt



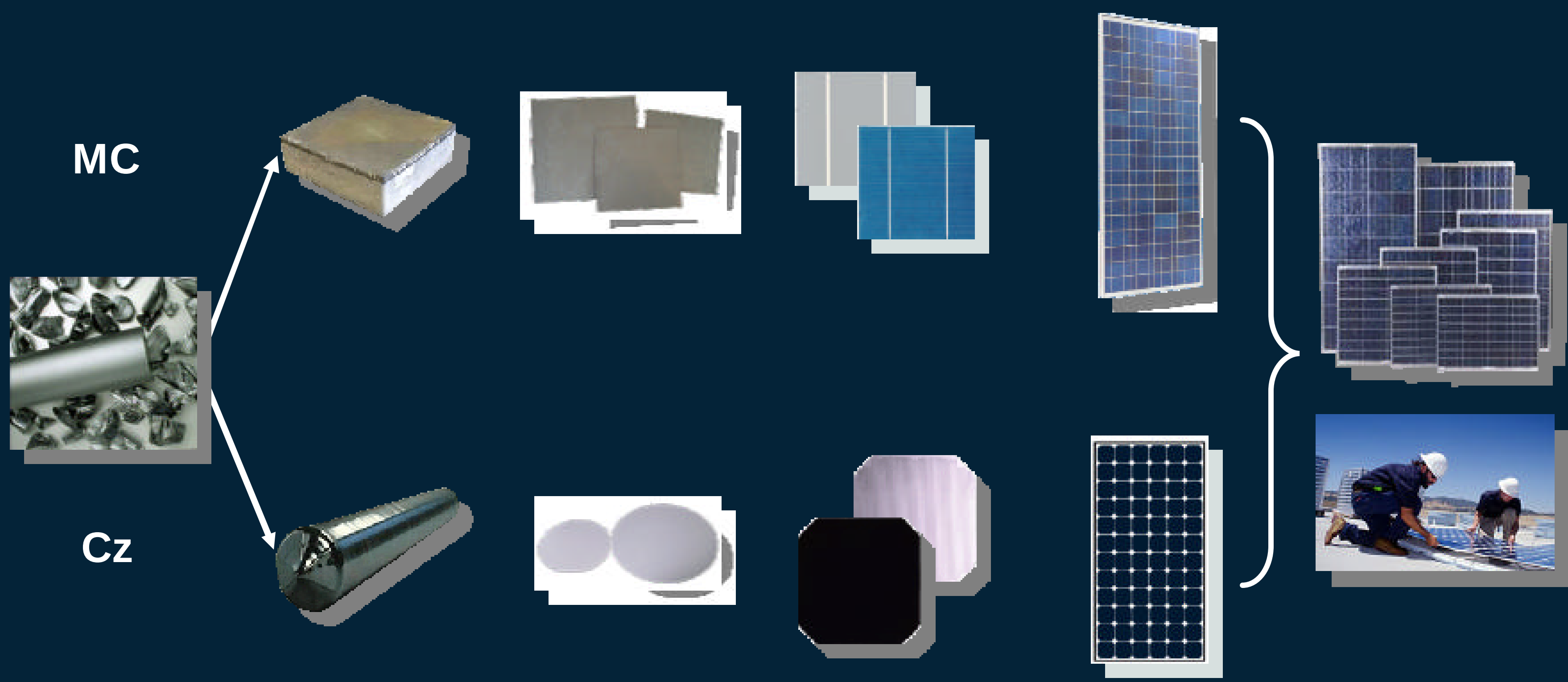
Production line size (Megawatts per Year)	**0.5** (1980)	**5** (2000)	**50** (2005)	**100** (2010)
Lines Per Factory	**2**	**3**	**4**	**10**

Source: Adapted from NREL

APPLIED MATERIALS

Crystalline Silicon PV Value Chain

Poly-Si Feedstock → **Ingot Production** → **Wafer or Sheet Production** → **Cell Production** → **Module Assembly** → **Distribution, Integration & Installation**



Improve Material Efficiency: Thin Wafers

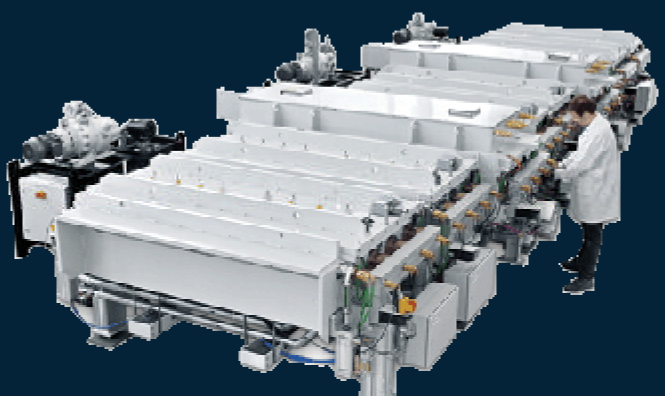
f Loss

/afer
ckness

$$\frac{\text{Cost / m}^2}{\text{Watt / m}^2}$$

* Cost assumes fixed silicon costs at $55/kg and constant efficiency

High Productivity ARC/Passivation



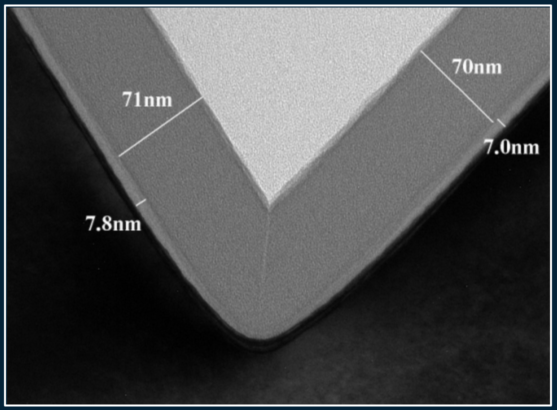
Applied ATON™ PVD

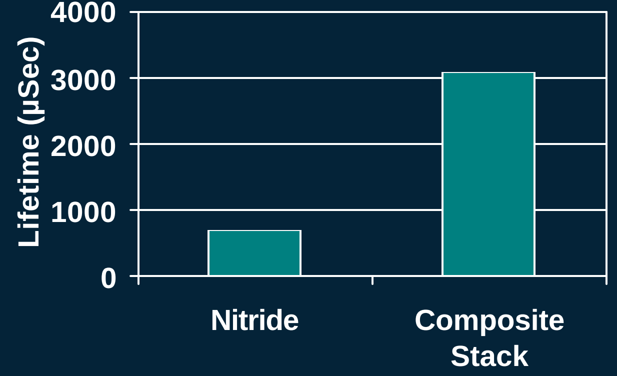
Cost / m^2

Watt / m^2

- Yield
- Thruput
- Uptime
- Thin wafers
- COC

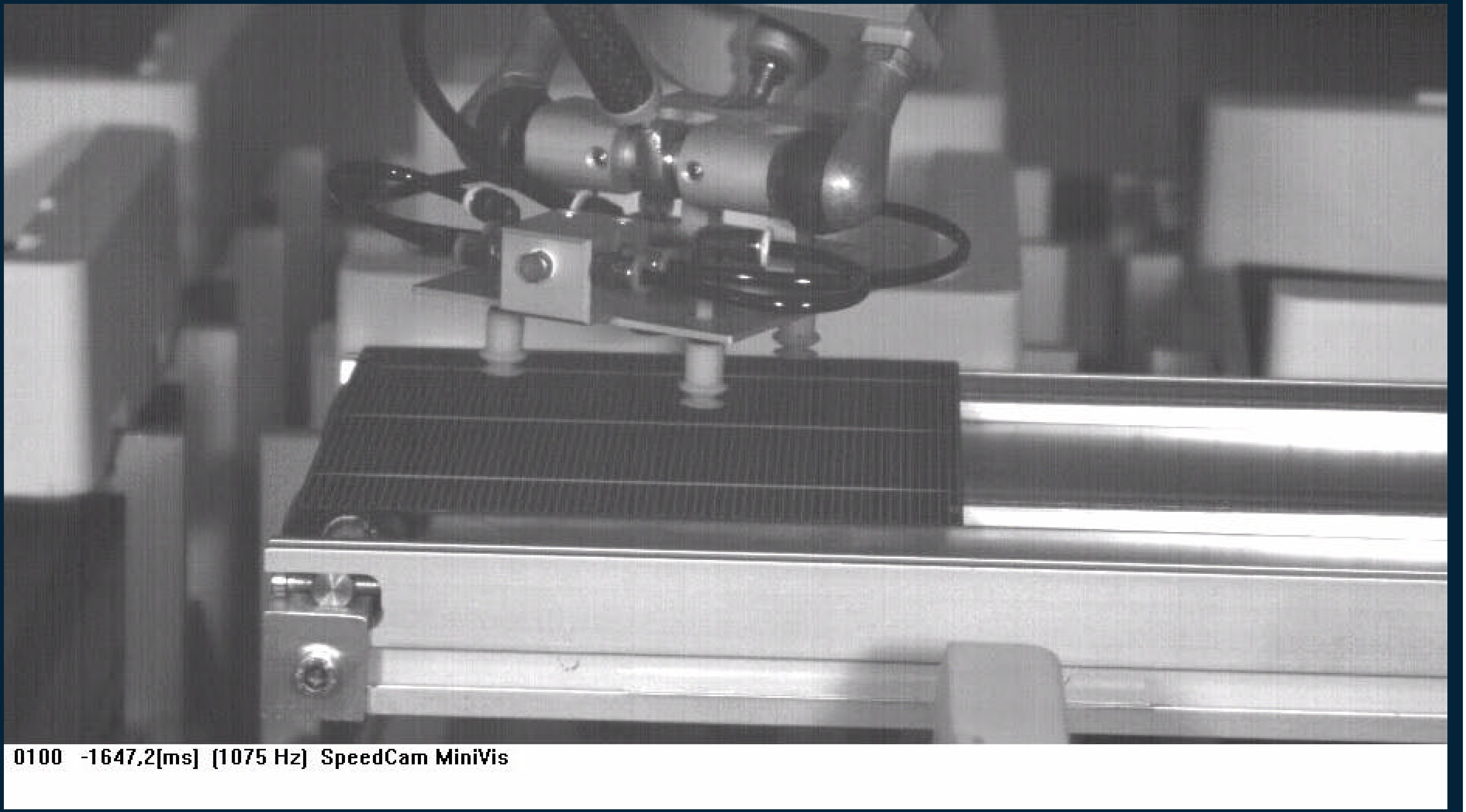
- Efficiency
- Uniformity





- **Low Interface State Density**
- **Optically Transparent**
- **Stable After Contact Firing**

Thin Wafer Processing



Thin Film PV Value Chain

Wafer or Sheet Production → Cell Production (Si, CdTe, CIS) → Module Assembly → Distribution, Integration & Installation