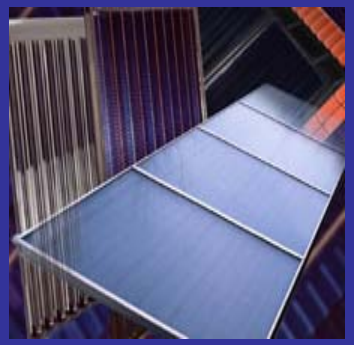
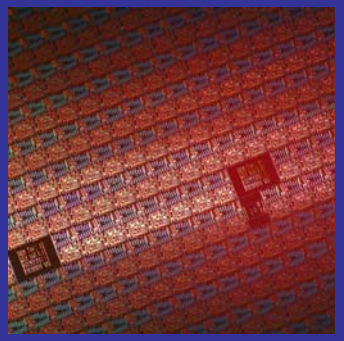
Continually cited as the model for a successful industry/government consortium

Accelerating the next technology revolution

The SEMATECH Model: Potential Applications to PV

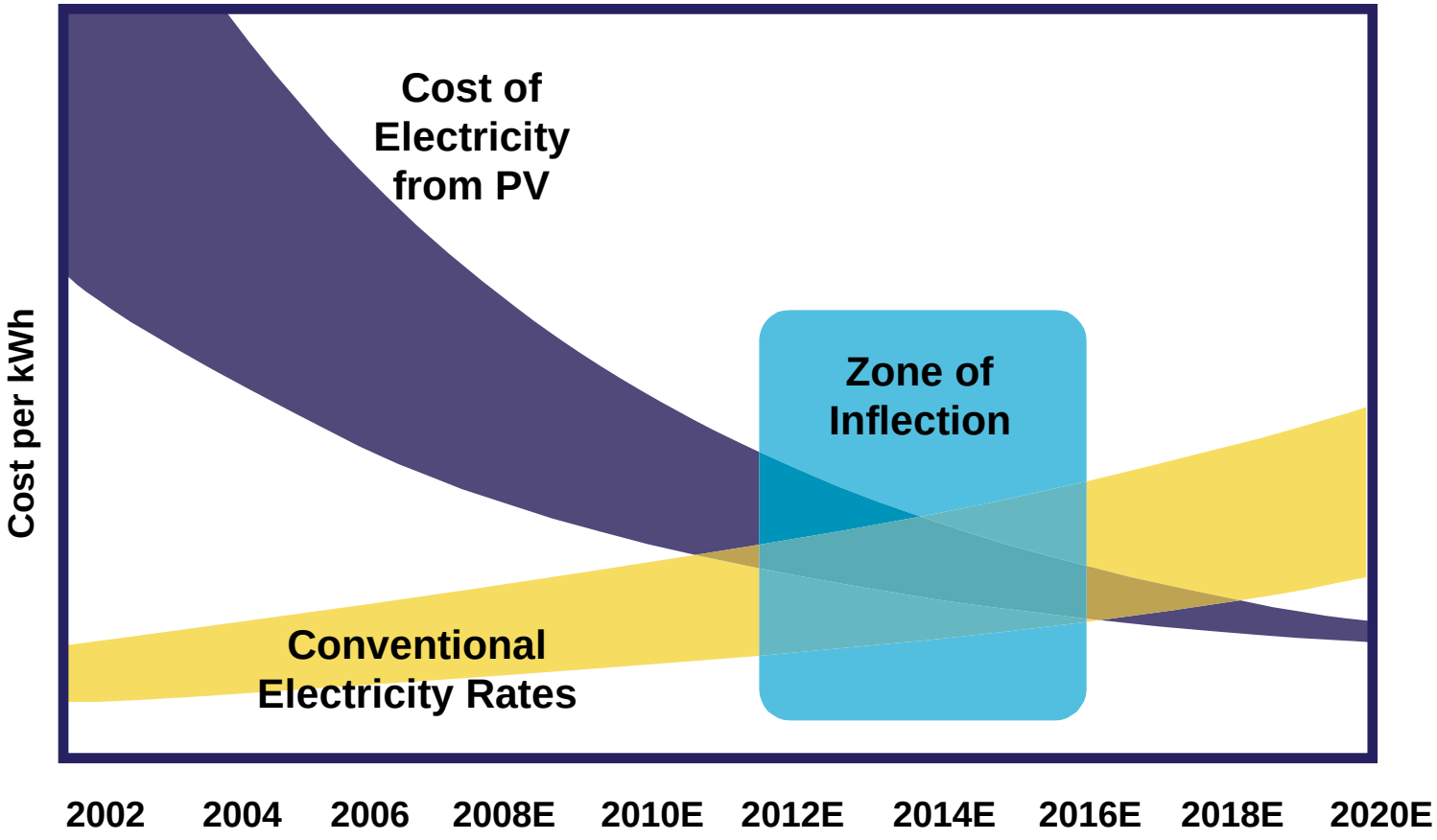


Dr. Michael R. Polcari
President and Chief Executive Officer
SEMATECH
National Academies, 29 July 2009

Solar grid parity convergence

How to apply the SEMATECH consortium model to reducing costs and driving PV manufacturing to grid parity



Solid State Technology, October 2008

Solar energy value chain

Driving technology innovation, productivity improvement and cost reductions across all segments

Materials → Equipment → Manufacturing Processes → Module Assembly → Balance of System → Installation

~35% total $ reduction for "grid parity"

SEMATECH is about semiconductor technology innovation and manufacturing productivity

Decrease cost per function

Technology Challenges

Increase transistors per area

- Lithography
- Metrology
- Devices
- Design
- Interconnects

Productivity Challenges

Cost per area

Cost per wafer

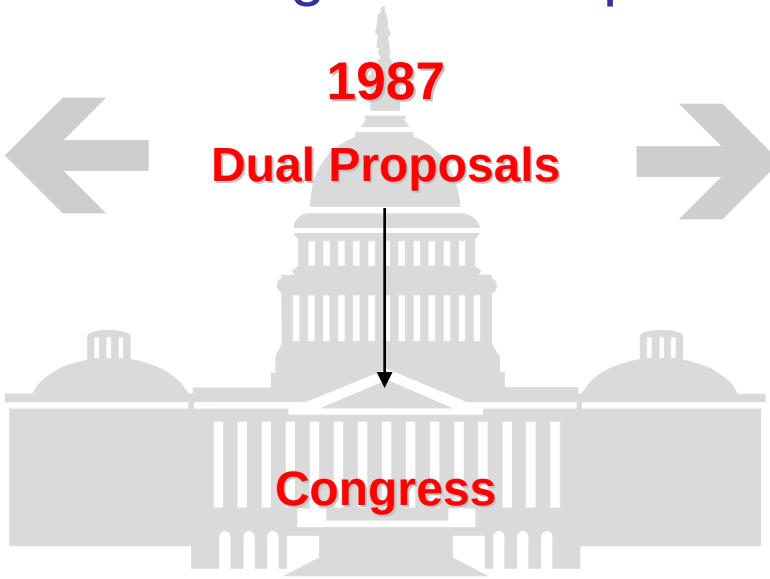
Area per wafer

Increase good wafer output

Reduce operating cost

Wafer size conversion

Government and industry agree SEMATECH needed to regain U.S. manufacturing leadership



Defense Science Board

Semiconductor Industry Association

1987

Dual Proposals

House Armed Services

House Science & Technology

Congress

Senate Armed Services

Senate Commerce

Public Law 100-180

$100M/year (+ $100M/year from Industry)

Department of Defense/Advanced Research Projects Agency

SEMATECH

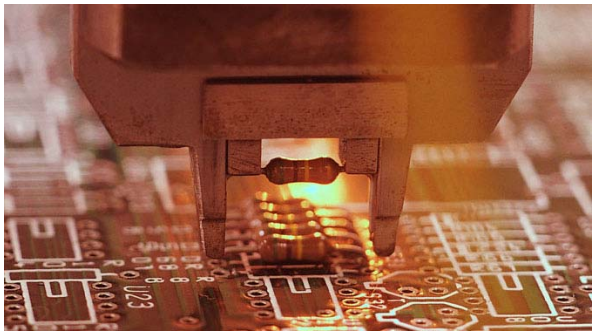
National not-for-profit consortium - five year "experiment" in public/private cooperation

SEMATECH successes

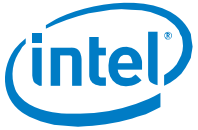
- Helped recapture US lead in semiconductors by mid-90's
  - Focus on improving, standardizing equipment/materials infrastructure
- Instrumental in establishing/maintaining semiconductor industry roadmap
- Led industry-wide initiatives to enable multi-billion dollar industry transitions
  - Next generation patterning – advanced technology development, equipment, materials (193nm dry immersion, EUV)
  - Next wafer size – Materials readiness, equipment performance metrics
  - Screening and characterization of new materials
    - >350 material systems for high-k metal gates, >500 low-k materials
- Explored "dry holes"
  - Cost avoidance for members/industry (157nm lithography)
- The SEMATECH Effect – job creation
- Average member ROI – 5.4x

SEMATECH success factors

- Commitment from top level executives, long-term support
  - Industry and government champions
- Industry leadership
  - Government-industry partnership
- A clear, pre-competitive mission
  - Accelerate commercialization by addressing common challenges, per industry roadmap
    - Building technology infrastructure
    - Strengthening manufacturing base
- Broad representation of industry, broad network of partners
  - Chipmakers and universities, national labs (Sandia, NIST), research institutes, equipment/materials manufacturers
- Leveraging of government and industry funds
- Member-driven organization
  - Company assignees



Worldwide collaboration
SEMATECH members



SEMATECH ecosystem

- More than 150 research partners around the world

Chip Makers

- IDMs
- Foundries
- Fabless
- Packaging

Universities

- Funded research
- New ideas and approaches

Governments

- National Labs
- Local economic Investments

Suppliers

- Equipment
- Materials
- Software

- Today, additional opportunities in emerging technologies
  - Many emerging technologies require silicon and consortial expertise
    - Solar, MEMS, sensors…

SEMATECH and semiconductor manufacturing productivity

- **The productivity challenge**
  - How to determine, achieve, and maintain world class fab productivity
  - How to increase productivity today and into the future
- **The cost reduction challenge**
  - How to continuously reduce costs in today's fabs
  - How to manage ever-increasing capital, manufacturing, and R&D costs
- **The sustainability challenge**
  - How to reduce our environmental footprint
    - Good for the environment, good for business

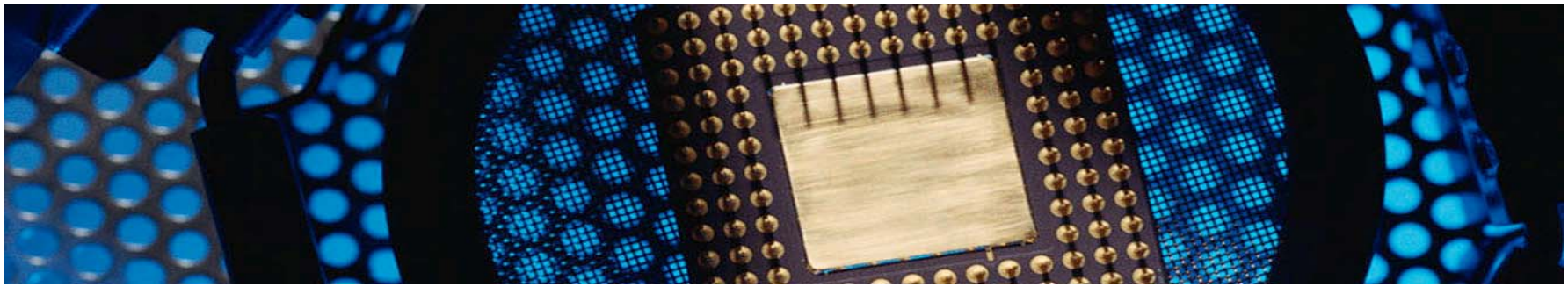
Tactical & strategic manufacturing solutions

WHAT

- Cost reduction
- Yield improvement
- Quality management
- Metrology
  - Defects, lithography, films
- ESH
  - Resource conservation
- Factories of the future
  - Factory automation
  - Next wafer size

HOW

- Fab benchmarking
- Equipment improvement teams
- Productivity workshops
- Operations/business councils
- Standards and roadmap development
- Materials screening, characterization

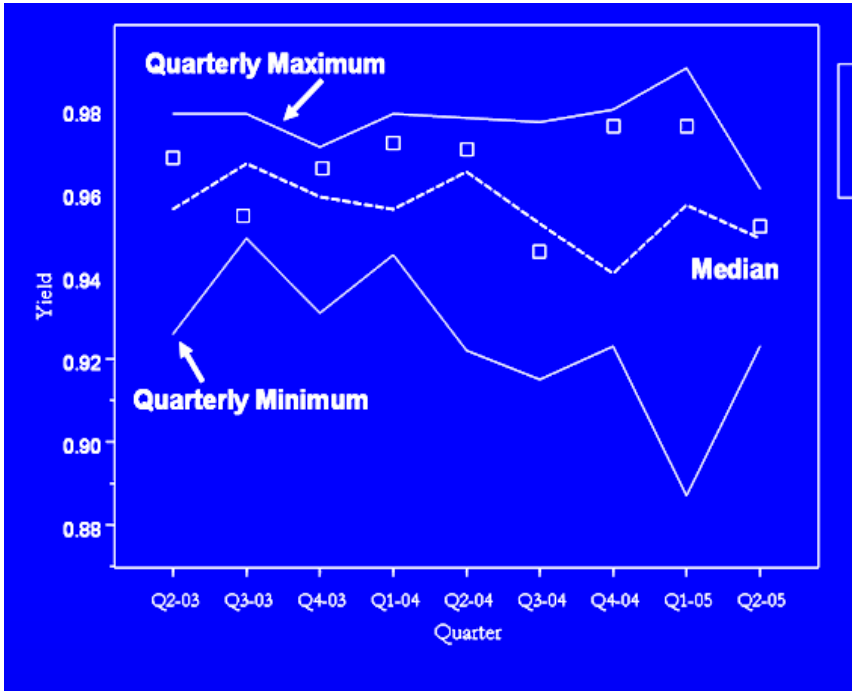


Councils

Benchmarking, surveys, best practices

- **Manufacturing Methods Council**
- **Quarterly fab metrics**
  - ~ 50 metrics reported
  - 20% productivity improvement in Members' wafer fabs over two year period
- **Special benchmarking topics per member request**

  Examples:
  - Gas and chemical cost
  - Maintenance cost

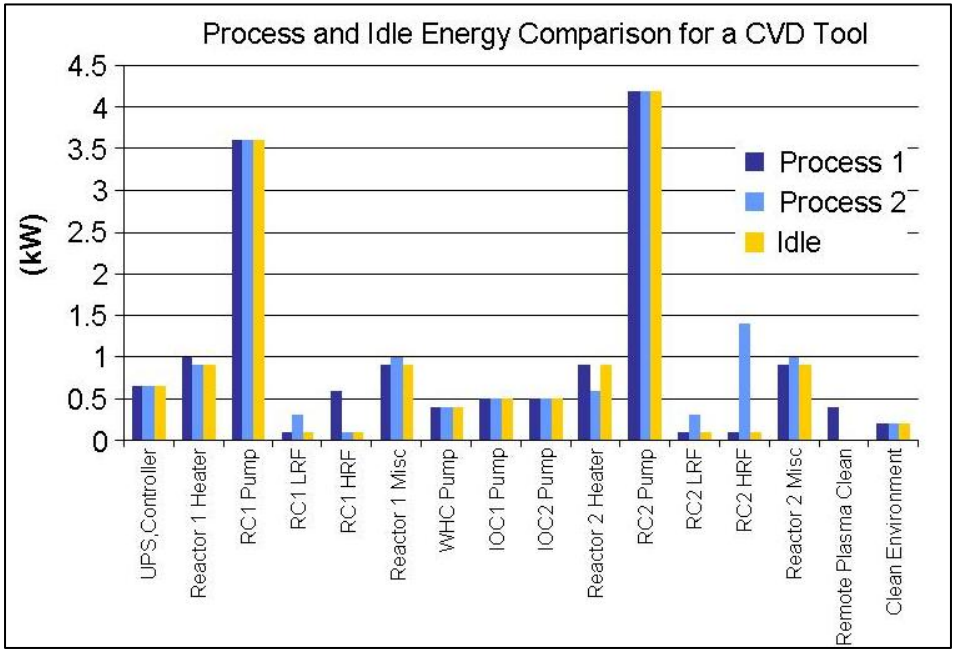


Average Wafer Line Yield Per 20 Layers

Energy and resource conservation

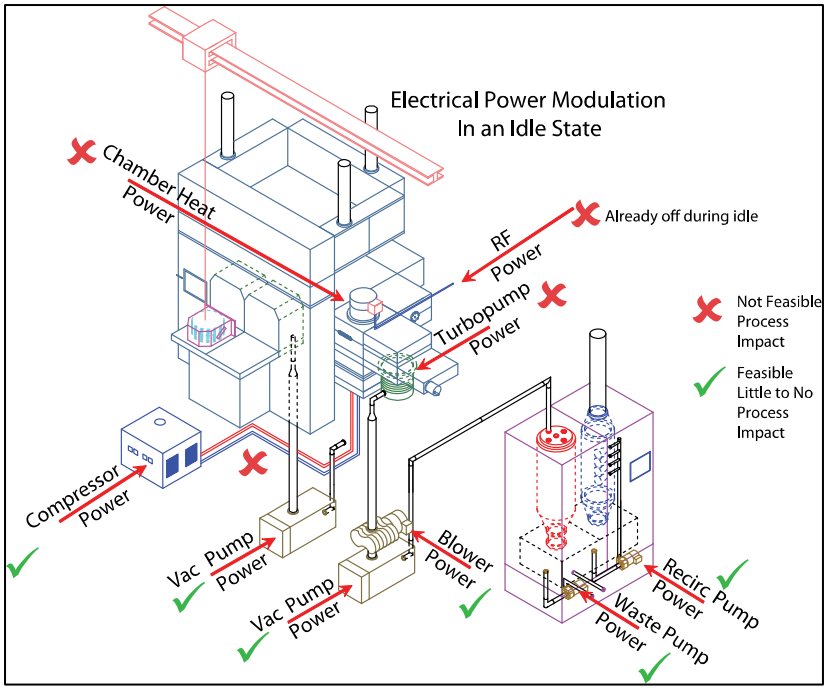
Survey

For nearly all process tool subcomponents, energy consumption is the same whether the tool is processing or idle



Component improvements

Reduced utility consumption - idle mode



Challenges identified in recent PV Roadmap Workshop

July 12, San Francisco (DOE/SEMI)

- Organizing collaborative platforms to address common industry challenges
- Establishing and maintaining a comprehensive roadmap
- Materials, technology and manufacturing standards
- Manufacturing productivity and overall cost reduction
- Equipment improvements
- Metrology development
- Test and certification
- Defectivity and materials characterization
- Environment, safety and health

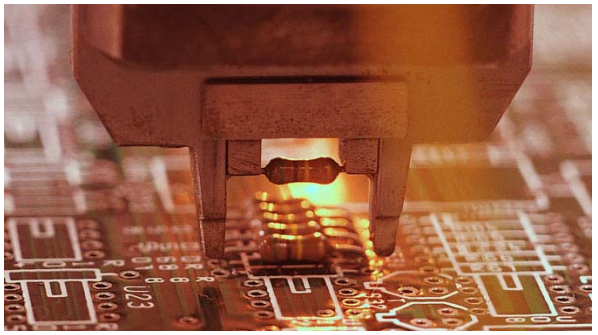
How SEMATECH can contribute to the PV industry

- Experience in:
  - **Technology development** to accelerate commercialization
    - Advanced/emerging technology R&D programs
  - **Manufacturing productivity** programs
    - Develop/harden manufacturing, metrology, and test equipment
    - ESH
  - **Collaborative strategies** to build consensus, guide industry direction
    - Roadmaps and standards
  - **Recruiting, organizing consortia**
    - Methodology for collaboration among competitors
    - Managing IP protocols
    - Coordinating programs between industry, national labs, and universities

Accelerating the next technology revolution

Research

Development



Manufacturing