NANOMANUFACTURING TECHNOLOGY

NAS/SSSC Spring Meeting
April 2, 2009
Moore's Law and Transistor Scaling

- Decrease transistor dimensions by k, drop voltage by k
- Circuit area reduced by 1/k^2, speed increased by k
- Power per circuit reduced by 1/k^2, power per area constant
Moore's Law and Transistor Cost

Number of Transistors (x Billions)

Cost per Transistor (Nano $)

(Source: G. Moore, ISSCC 2003)
A Recent Product Enabled by Nanoelectronics

1975 = $1B†
2006 ~ $200
2020 = 5¢*

† Memory cost only
* Extrapolating memory cost reduction factor over last 30 years and display cost/area over last 10 years
Cost Per Function

Cost
Function

Process Cost
Area

(Good) Function
Area
Cost Per Function: VLSI Technology

Scaling has been the primary cost driver for ICs – but not at an overcompensating increase in process cost/area.
Patterning Is More Than Printing

**PREPARATION**
- Patterning Films
  - CVD Hardmask
  - CVD ARC/Spin-on ARC
  - PVD Hardmask
- Planarity Enhancement
  - Ecmp
  - Real-Time Profile Ctrl
  - Fixed-Abrasive CMP

**PRODUCTIVITY**
- Automation
- eDiagnostics
- Material Handling
- Reticle Management

**PRINTING**
- Scanner
- Track
- Mask/Mask Etch
- Photoresist
- K₁ reduction

**PROCESS CONTROL/DFM**
- CD SEM
- OPC Qualification
- APC
- Defect Inspection and Review
- Overlay

**PATTERN TRANSFER**
- Etch
  - High Aspect Ratio Etch
  - Critical Etch
  - Damascene Etch
  - Trimming
Self Aligned Double Patterning

1. Pattern Photoresist
2. Trim Photoresist
3. First APP Etch
4. Create Dielectric Spacer
5. Etch Dielectric Spacer
6. 32nm Line/Space Array Made with 128nm Pitch on 193nm Dry Line

LER = 3.1nm (3σ) after lithography

LER = 1.5nm (3σ) after final APF etch
Progress Through Materials Innovation

Source: Intel – ISTAC Meeting 2-2004
Integrated Hi-k/Metal Gate CMOS

- Metal Gates for nMOS and pMOS
- Hi-K layer for low leakage
- High mobility interface layer
- Graded transition layer

**Diagram:**
- DHx Nitridation
- High-k Dielectric
- Radiance± Oxidation
- Radiance± Anreal
- PVD Metal Gate
- ALD/PVD Metal Gate
- Dual Mode Depsas
- AdvantEdge® G3 Poly/metal gate etch
- Cadima® High-Temperature High-ketch
- Axiom® Habogen abatement Strip and passivation
Require Nanoscale Resolution *and* Throughput

**Critical Defect Size (nm)**

- 1994
- 1997
- 1999
- 2001
- 2003
- 2005

**Defects Reviewed Per Day at a Leading Fab**

- 1996
- 1998
- 2000
- 2002
- 2004

**Throughput (300mm WPH)**

- New Tool
- Existing Tool

**Pixel** = 80nm, 120nm, 160nm, 220nm, 270nm

35nm void
30nm defect
Two Key Semiconductor Market Trends

Semiconductor content in electronics, units and transistors all continue to increase but:

- Accelerated consolidation of wafer manufacturers
  - Foundries vs. IDMs
  - Memory oversupply
  - Process R&D costs

- Fewer product families aggressively follow Moore's law
  - Application drivers
  - Developing economies
  - Performance compromises
  - Design costs
Promise of Nanotechnology

- Nano-particle paint to prevent corrosion
- Thermo-chromic glass to regulate the influx of light
- Organic Light Emitting Diodes (OLEDs) for displays
- Photovoltaic film that converts light into electricity
- LEDs are now powerful enough to compete with light bulbs
- Scratchproof, coated windowpanes using the Ions effect
- Menu card made of electronic cardboard
- Nanobes for new notebook displays
- Fabrics coated to resist stains
- Prezoms prevent annoying vibrations
- Hip joints made from biocompatible materials
- The helmet maintains contact with the wearer
- Intelligent clothing measures pulse and respiration
- The Bucky-tube frame is as light as a feather, yet strong
- Fuel cells provide power for mobile phones and vehicles
- Magnetic layers for compact data memory

Nanomanufacturing Technology
Small features on a large production scale

Placing a nanotube?

Scale Up?

Additional Innovation

More Than Nanofabrication – Repeatable, Robust, Reliable, Controllable and Cost Effective
Flat Panel Display (LCD) Manufacturing

> 20% Bigger (HD)TV Every Year for the Same Price
Cost per area tends to be an equivalent or predominant factor in applications other than VLSI.
Flat Panel Display Equipment – PECVD

<table>
<thead>
<tr>
<th>Model</th>
<th>Substrate</th>
<th>Size (mm)</th>
<th>Area (cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gen 2</td>
<td>2,000</td>
<td>(1.00)</td>
<td></td>
</tr>
<tr>
<td>Gen 3 / 3.5</td>
<td>4,650</td>
<td>(2.33 from 1600)</td>
<td></td>
</tr>
<tr>
<td>Gen 4</td>
<td>6,716</td>
<td>(1.44 from 4300)</td>
<td></td>
</tr>
<tr>
<td>Gen 5</td>
<td>12,000</td>
<td>(1.79 from 5500)</td>
<td></td>
</tr>
<tr>
<td>Gen 5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gen 5.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gen 6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gen 7 / 7.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gen 8</td>
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</tbody>
</table>

Gen 10 = 60nm uniformity over ~ $10^{19}$ nm² area at 50sph
Nanotechnology Opportunities In Energy

Energy Conservation

Energy Conversion

Energy Storage

Technology to improve performance, form and cost
Architectural Coated Glass

Cost Reductions Achieved with Low-e Coatings

2000 ft² house with 300 ft² of windows
Increasing Adoption of Coated Glass

Bird’s Nest Stadium (Beijing)
Shanghai SYP Engineering Glass Co.
10,000m² of high performance Low-E glass

Burj Dubai (UAE)
Guardian Industries
100,000m² SunGuard® Solar Control and Low-E coated glass

Main Triangle Building (Frankfurt)
Guardian Industries
15,000m² SunGuard® Solar Control and Low-E coated glass

House of Sweden (Washington DC)
AGC Flat Glass
5500m² Stopray® Elite and Stopray® Carat glass

Savings from 2007 Global Output ~ 36,000 Bbl/day†

† Equivalent to 12 oil wells or 18Mt CO₂
Large Area Glass Coating Systems

- Glass Substrate is ~ 2.6 m x 3.6 m
  - Uniformity Spec of +/- 1% on 275 nm film (10 layer Triple Low e stack)
- 18 Chamber System ~ 90m: one panel every 20 sec
  - Output per month ~ 7Mft²
Electrochromic "Smart Glass"

Key Requirements for Market Adoption:
- **Performance**: Energy efficiency, lifetime
- **Form**: Color selection, match non-EC panes, pane-to-pane consistency, large size panes, on-off
- **Cost**: At least comparable to Low-e glass + shades

**Typical Structure**
- ~ 10 metal/dielectric layers, most < 100nm thick (up to ~ 500nm)

Images courtesy of Sage Electrochromics
Primary Commercial Solar PV Markets

Today’s Installed Base
5.4 GW

Market Drivers
- High utility bills
- Availability of incentives
- Green choice

Today’s Installed Base
4.2 GW

Market Drivers
- High utility bills
- Unpredictable cost
- Under-utilized urban space

Today’s Installed Base
5.4 GW

Market Drivers
- Solar economics
- Favorable tax policy
- Unpredictable fuel and carbon costs

Total new PV installations in 2008 ~4.1 GW

Mainstream PV Technologies

**Crystalline Silicon**
Preferred for residential applications

**Thin Film**
Preferred for large scale applications

Common focus to drive down cost per watt
Solar Learning Curve: Module Cost/Watt

$1.00/W @ <20 GW

$1.00/W @ >100 GW

Historical Prices (cSi dominated)

Production line size (Megawatts per Year)
- 0.5 (1980)
- 5 (2000)
- 50 (2005)
- 100 (2010)

Lines Per Factory
- 2
- 3
- 4
- 10

Cumulative Production (MWp)

Cost

Watt

= Cost / m²

Watt / m²

Source: Adapted from NREL
Crystalline Silicon PV Value Chain

Poly-Si Feedstock → Ingot Production → Wafer or Sheet Production → Cell Production → Module Assembly → Distribution, Integration & Installation

MC

Cz

Distribution, Integration & Installation
Improve Material Efficiency: Thin Wafers

- Cost / m²
  - $0.52 / Wp*
  - $0.46 / Wp*
  - $0.42 / Wp*
  - $0.34 / Wp*

- Kerf Loss (assuming fixed silicon costs at $55/kg and constant efficiency)
  - Wafer Thickness
    - 200
    - 180
    - 150
    - 120

* Cost assumes fixed silicon costs at $55/kg and constant efficiency
High Productivity ARC/Passivation

- Yield
- Thruput
- Uptime
- Thin wafers
- COC
- Efficiency
- Uniformity

- Low Interface State Density
- Optically Transparent
- Stable After Contact Firing

Applied ATON™ PVD

Cost / m²

Watt / m²

Nitride Composite Stack

<table>
<thead>
<tr>
<th>Lifetime (µSec)</th>
<th>Nitride</th>
<th>Composite Stack</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>4000</td>
<td>3000</td>
</tr>
<tr>
<td></td>
<td>3000</td>
<td>2000</td>
</tr>
<tr>
<td></td>
<td>2000</td>
<td>1000</td>
</tr>
</tbody>
</table>

0 1000 2000 3000 4000

71nm

7.0nm

7.8nm
Thin Wafer Processing
Thin Film PV Value Chain

- **Wafer or Sheet Production**
- **Cell Production (Si, CdTe, CIS)**
- **Module Assembly**
- **Distribution, Integration & Installation**

[Images of production processes]